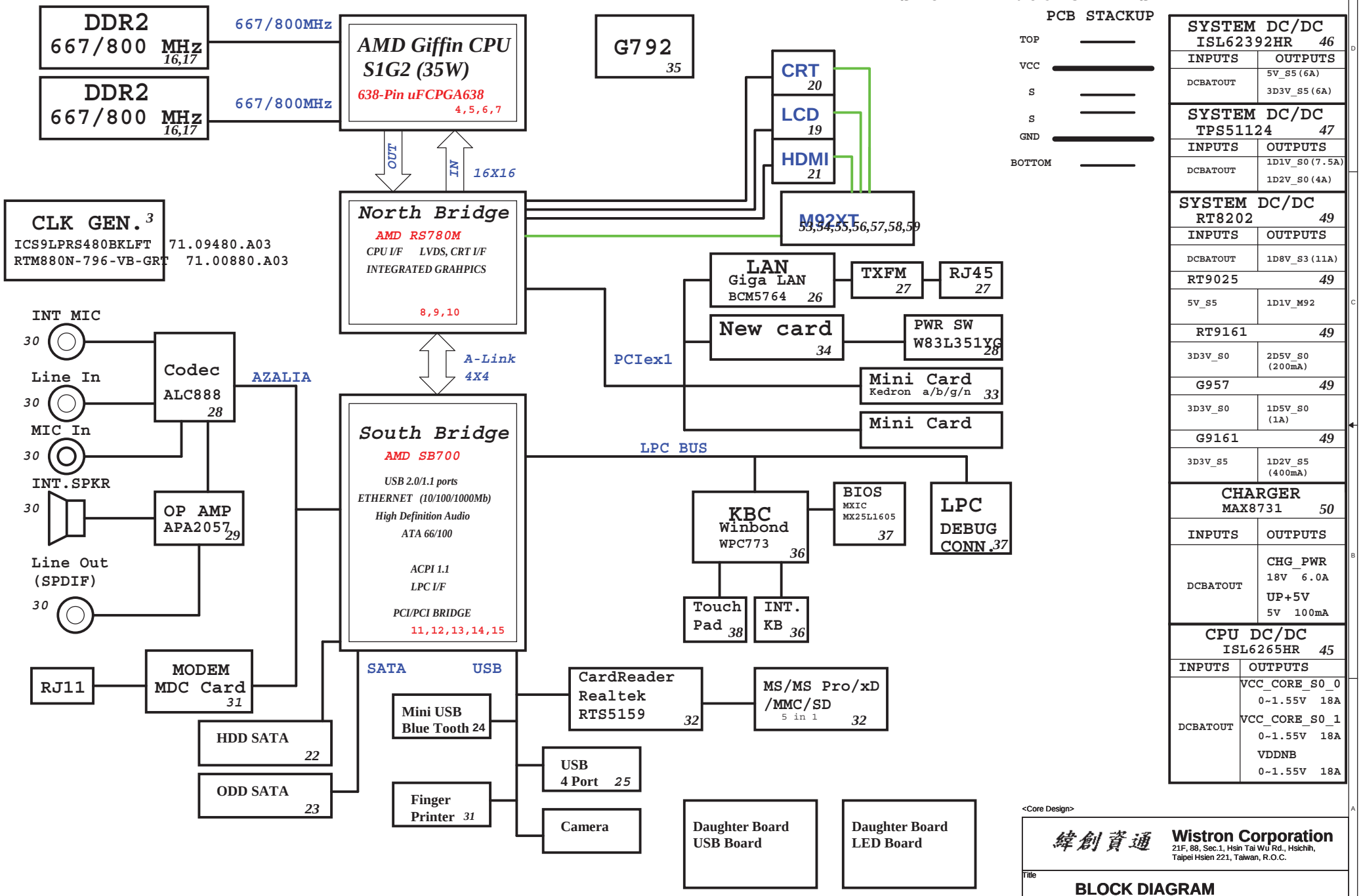
JV50-PU Block Diagram

Project code: 91.4CH01.001
PCB P/N : 48.4C901.001
REVISION :08252- -SB



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC ISL62392HR 46	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(6A)

SYSTEM DC/DC TPS51124 47	
INPUTS	OUTPUTS
DCBATOUT	1D1V_S0(7.5A) 1D2V_S0(4A)

SYSTEM DC/DC RT8202 49	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3(11A)
RT9025 49	
5V_S5	1D1V_M92
RT9161 49	
3D3V_S0	2D5V_S0 (200mA)
G957 49	
3D3V_S0	1D5V_S0 (1A)
G9161 49	
3D3V_S5	1D2V_S5 (400mA)

CHARGER MAX8731 50	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265HR 45	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: A3 | Document Number: JV50-PU | Rev: SB
Date: Friday, December 19, 2008 | Sheet 1 of 61

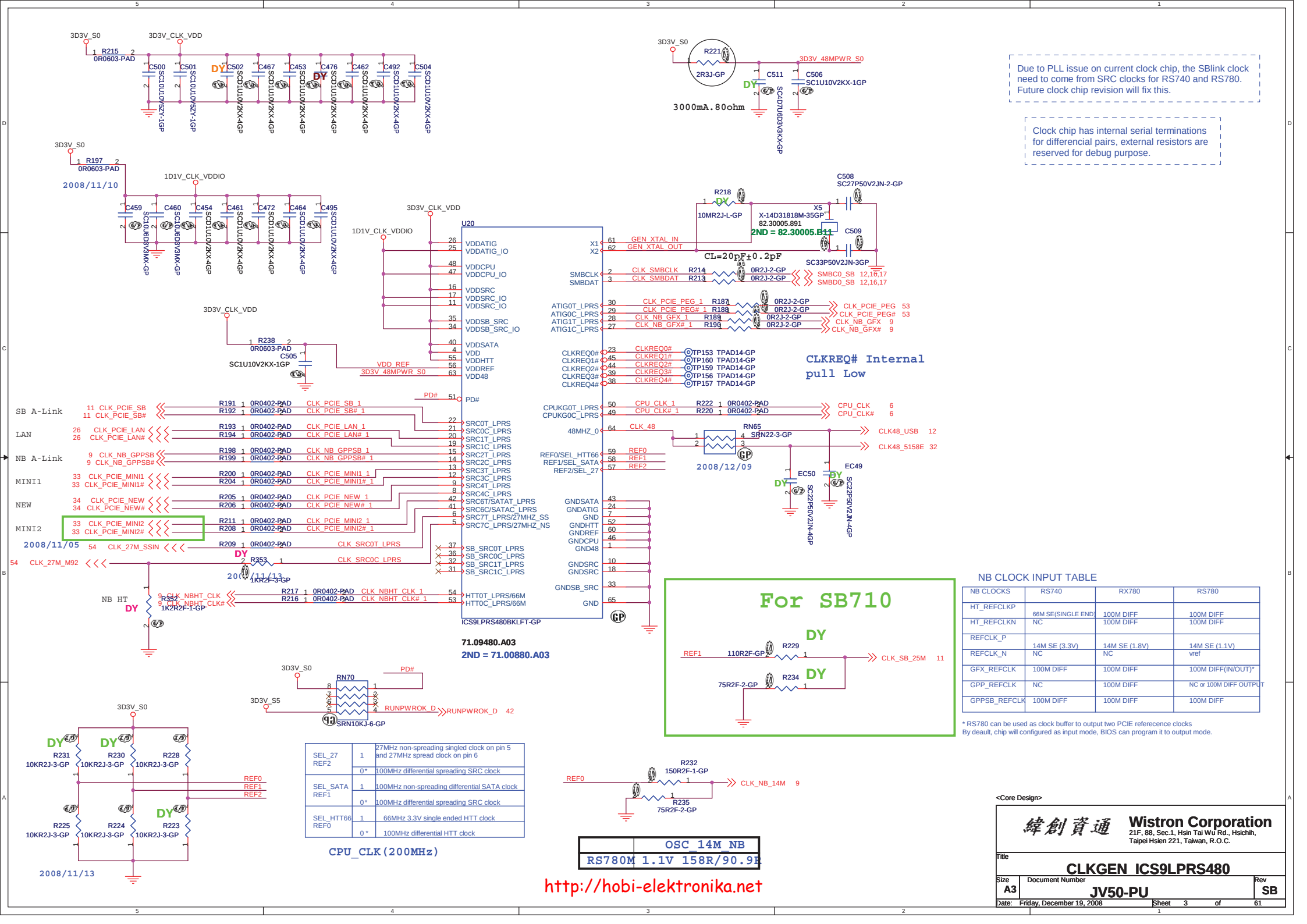
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB/PCIE Routing**

Size	Document Number	Rev
A3	JV50-PU	SB

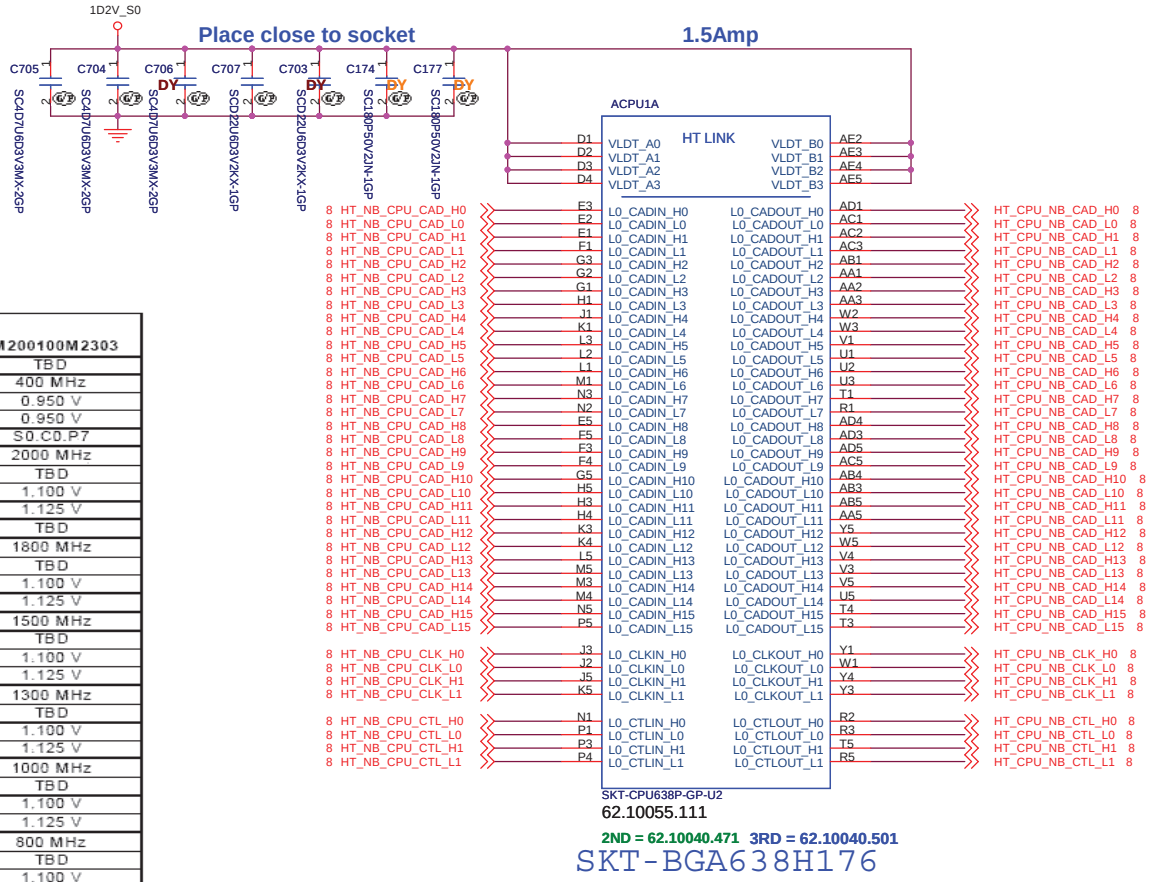
Date: Friday, December 19, 2008 Sheet 2 of 61



NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIE referecence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

SEL_27 REF2	1	27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
	0 *	100MHz differential spreading SRC clock
SEL_SATA REF1	1	100MHz non-spreading differential SATA clock
	0 *	100MHz differential spreading SRC clock
SEL_HTT66 REF0	1	66MHz 3.3V single ended HTT clock
	0 *	100MHz differential HTT clock



State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

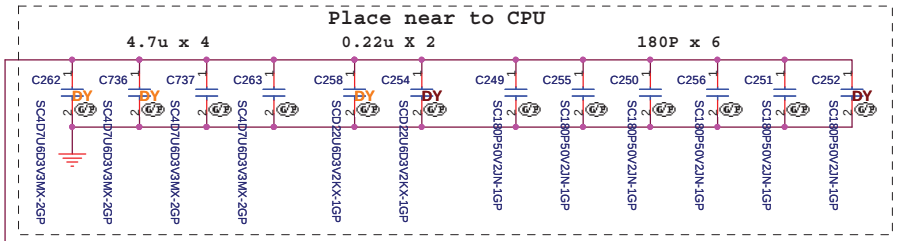
<Core Design>

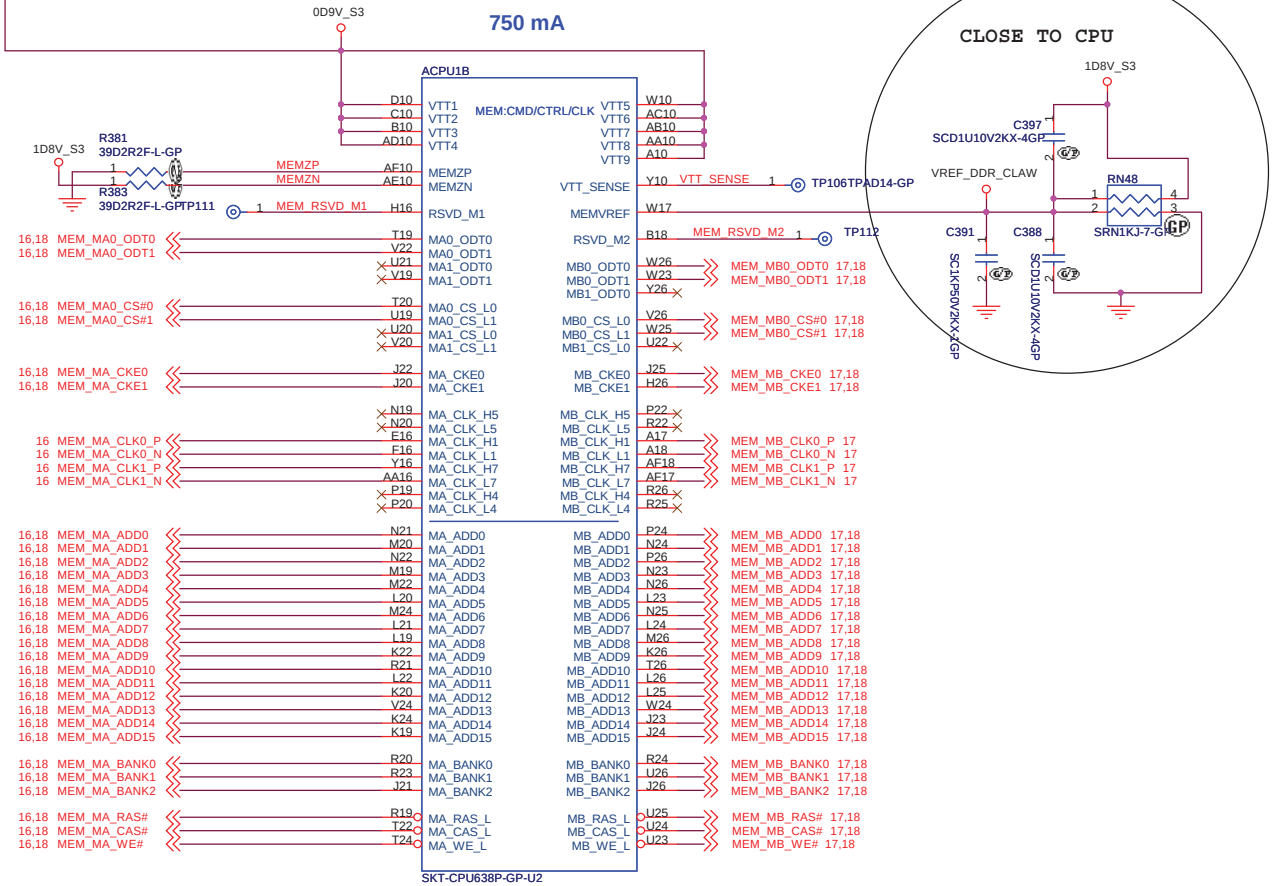
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

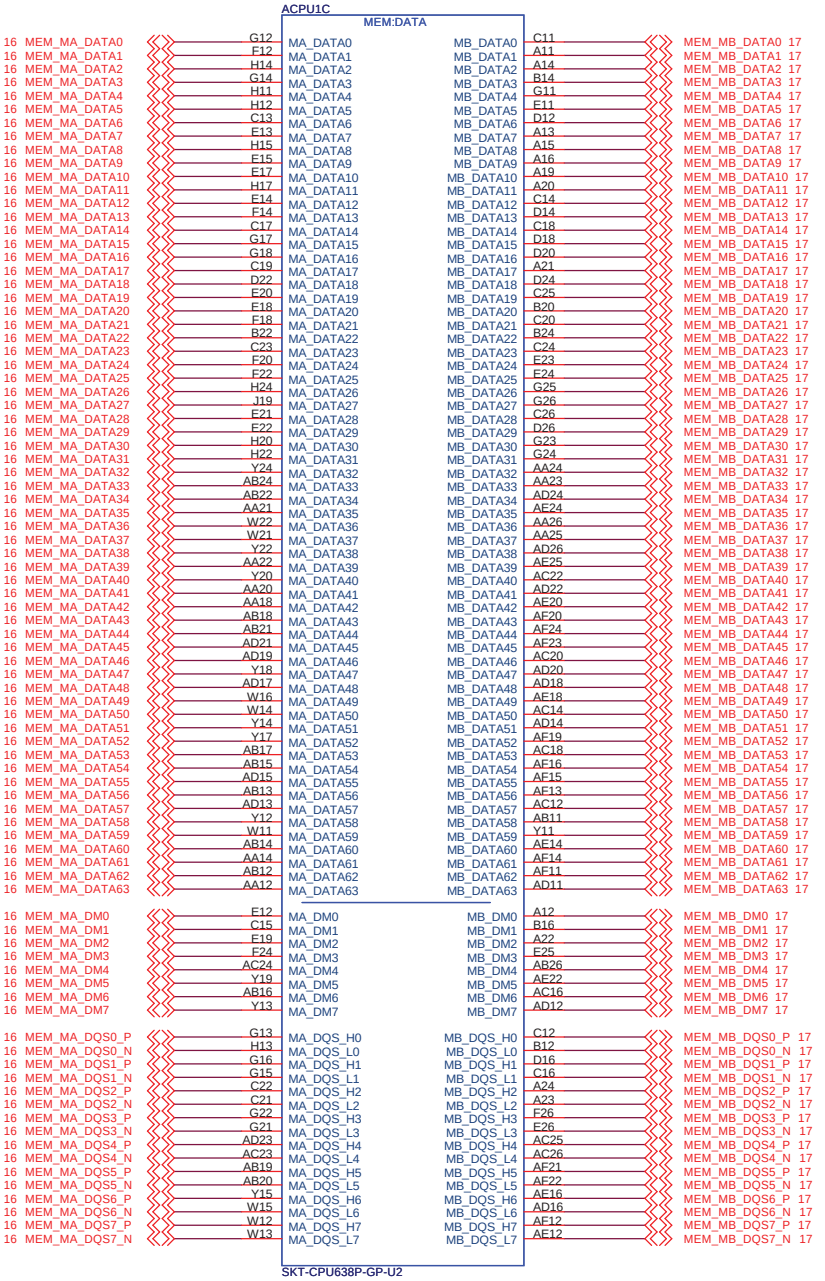
Title: CPU HT LINK I/F (1/4)

Size: A3 | Document Number: JV50-PU | Rev: SB

Date: Friday, December 19, 2008 | Sheet 4 of 61







<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_DDR_(2/4)

Size: A3 | Document Number: JV50-PU | Rev: SB

Date: Friday, December 19, 2008 | Sheet 5 of 61

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

Cloce To CPU

For HDT DBG

internal pull high 300 ohm

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

For leverage S1g3, please reserve 300 ohm resistor pullup to VDDIO.

For leverage S1g3, please reserve 300 ohm resistor pulldown to VSS

SA

Near CPU PIN

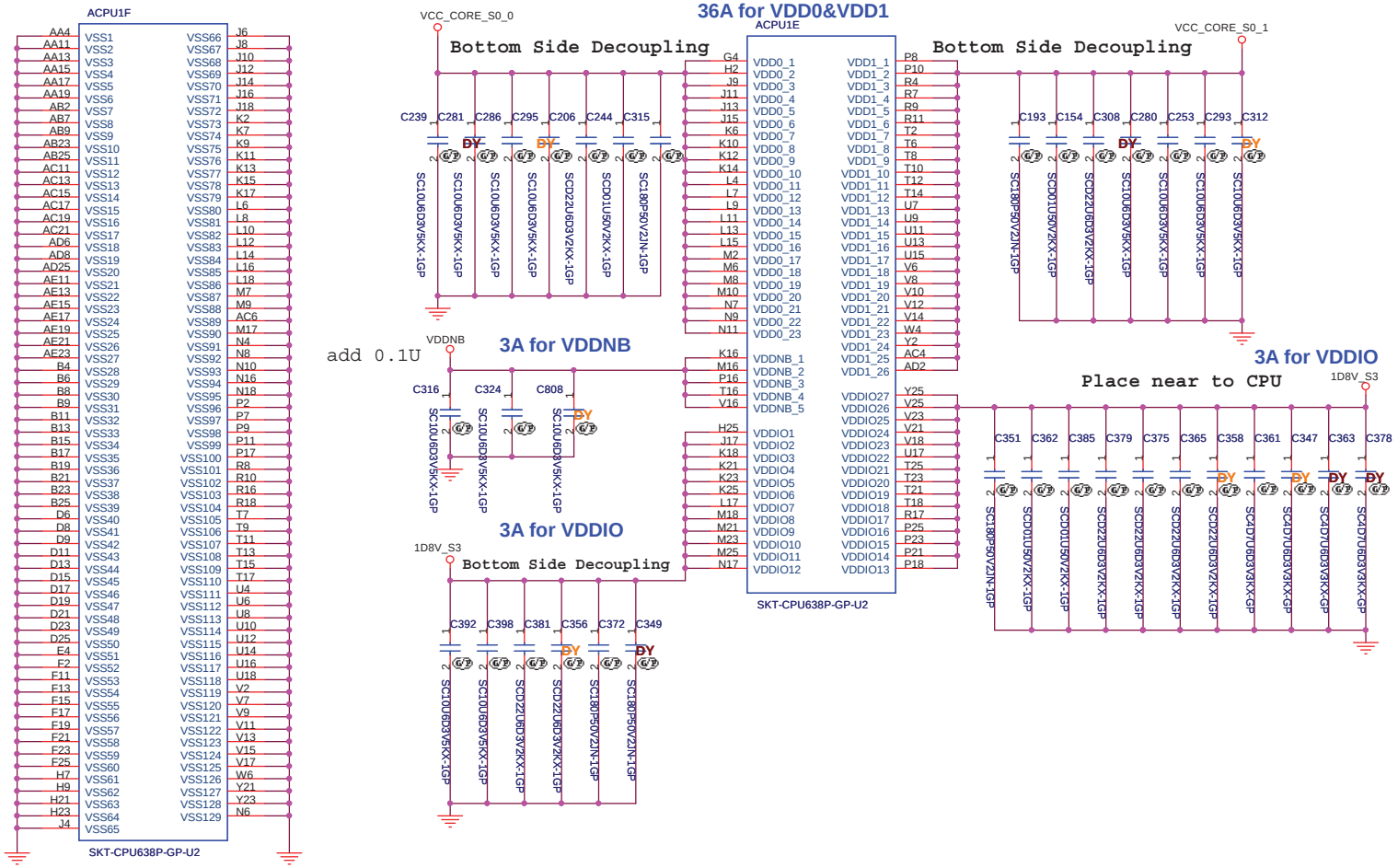
CPU exceeds to 125℃

SKT-CPU638P-GP-U2

HDT Connectors

<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CPU_Control&Debug_(3/4)	
Size A3	Document Number JV50-PU	Rev SB
Date: Friday, December 19, 2008	Sheet 6 of 61	

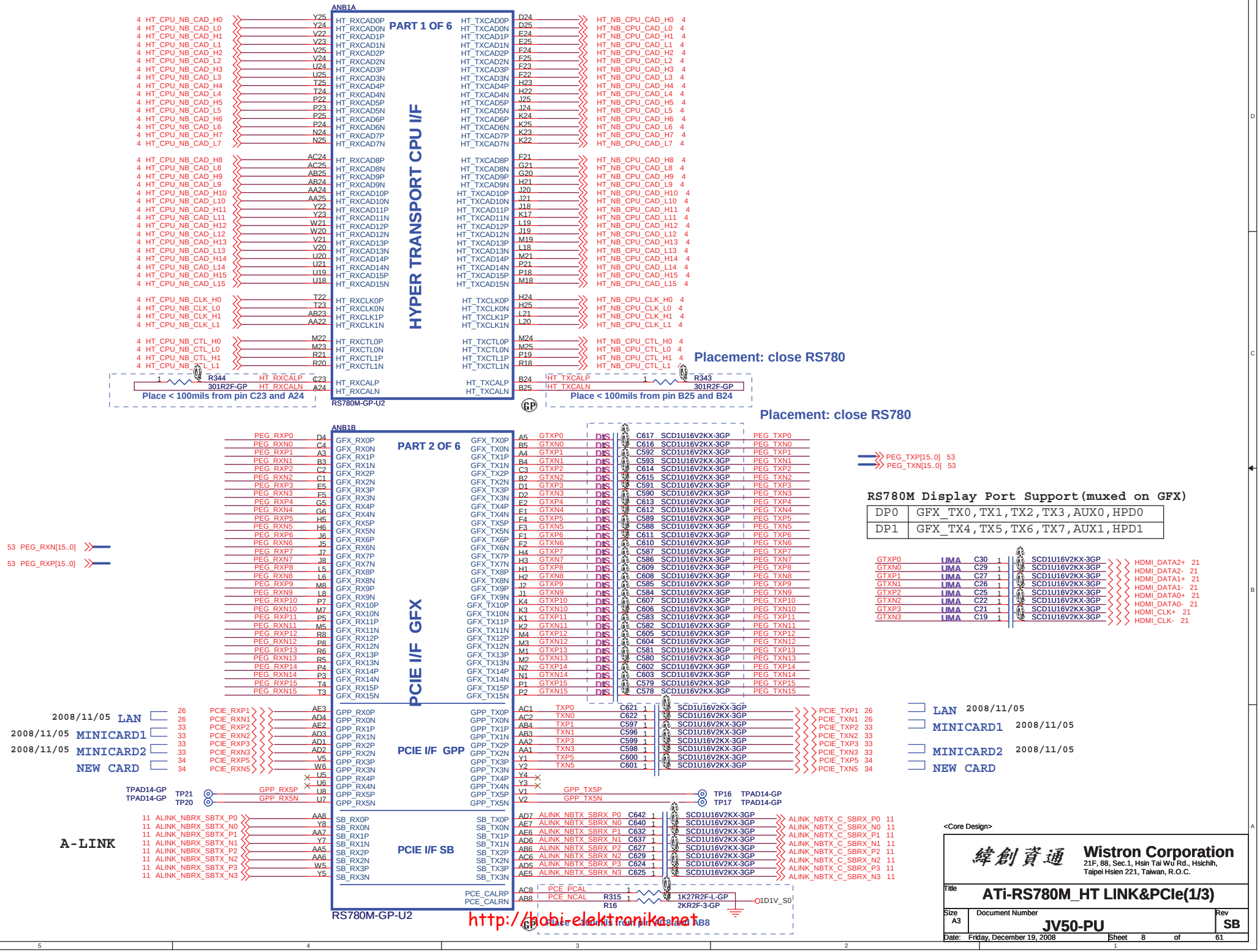


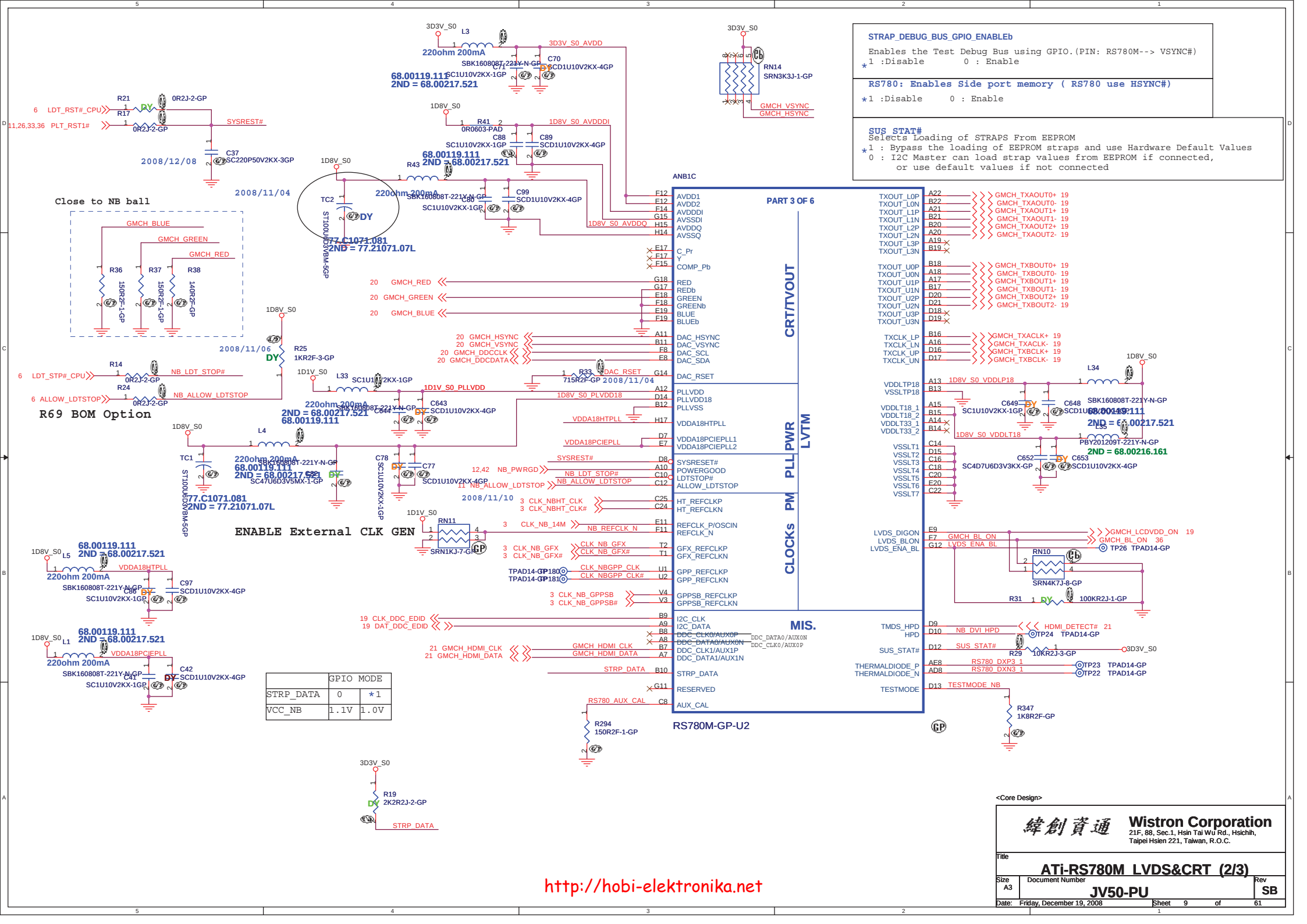
http://hobi-elektronika.net

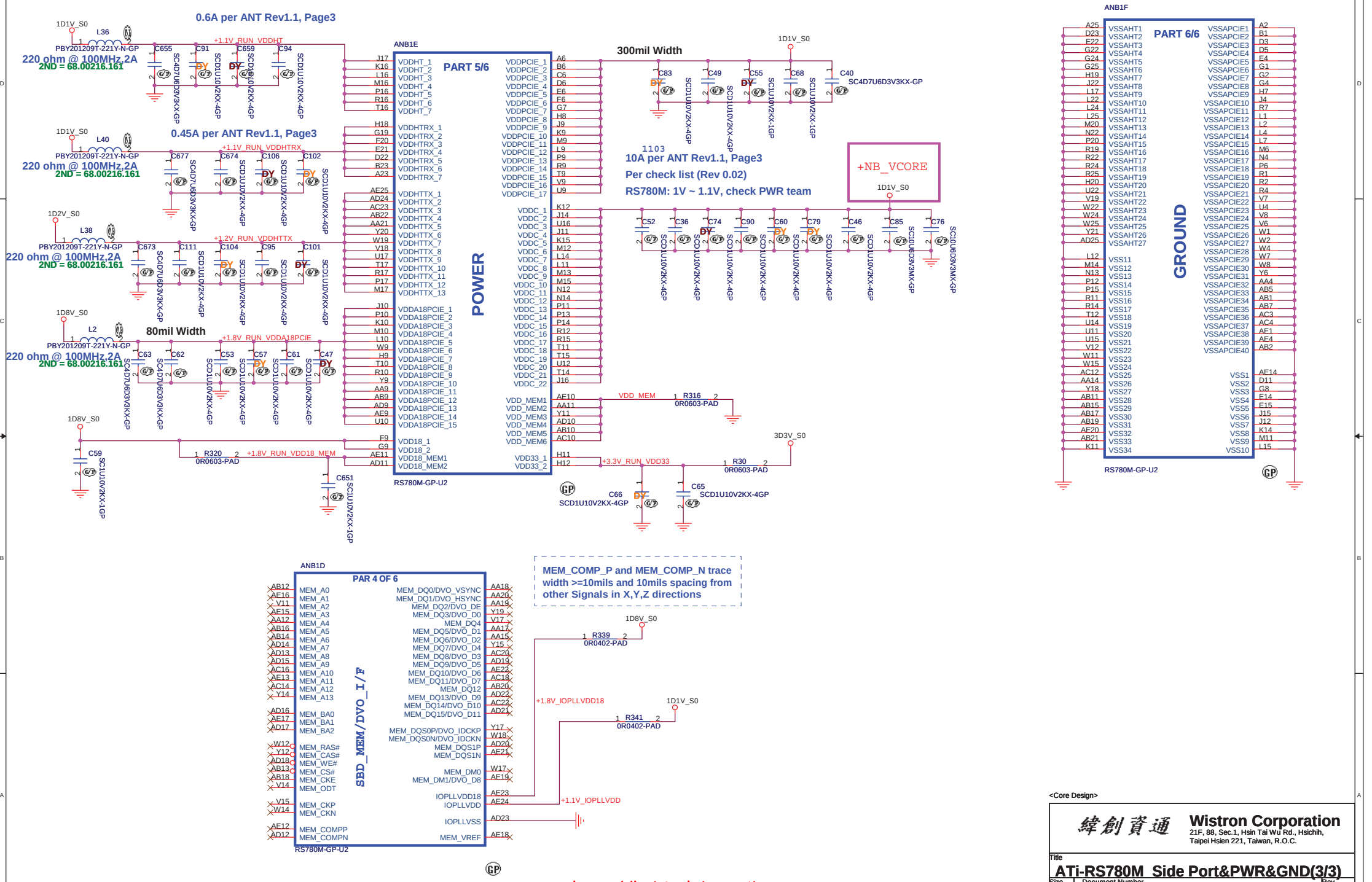
<Core Design>

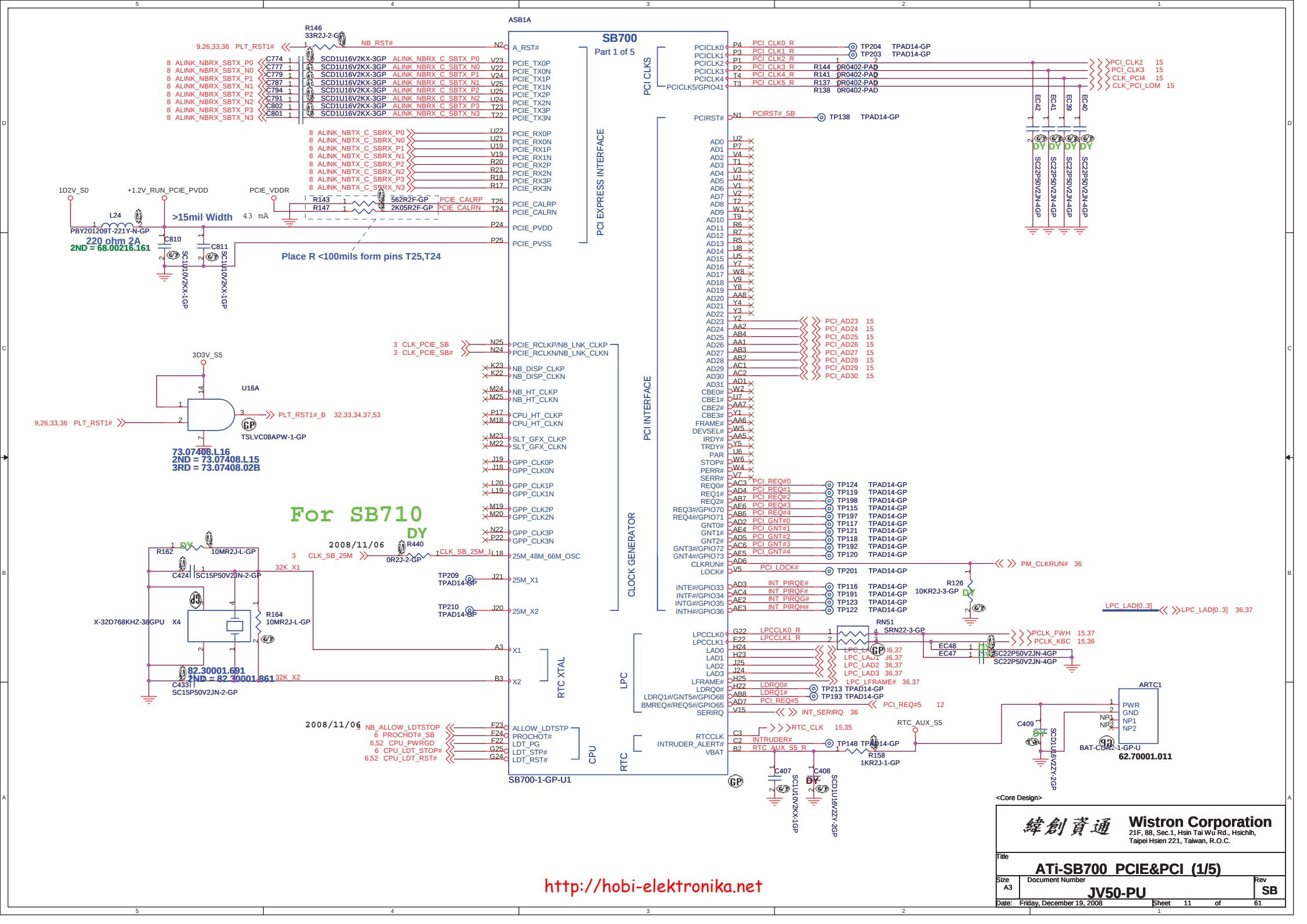
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

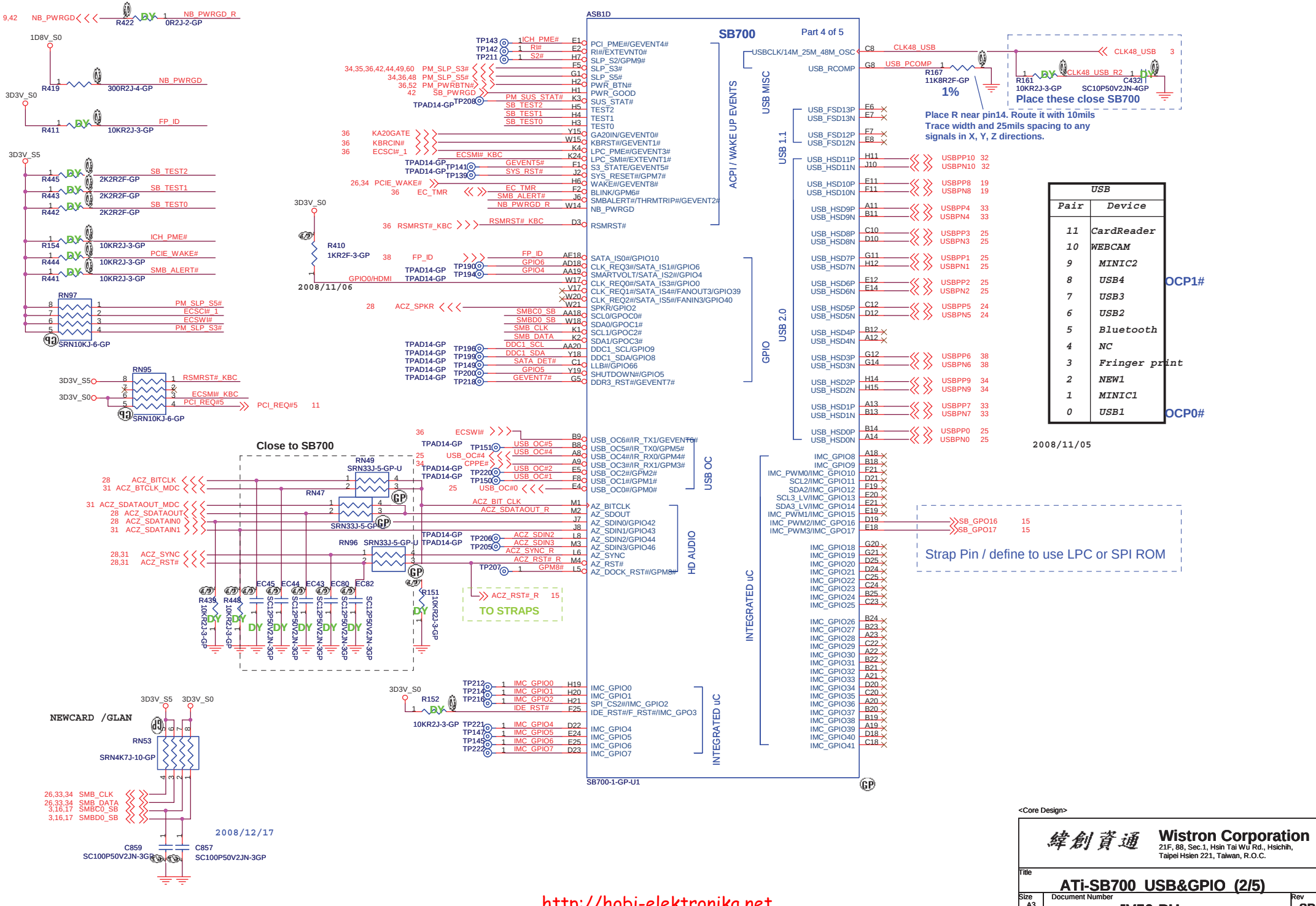
Title	CPU_Power_(4/4)	
Size A3	Document Number JV50-PU	Rev SB
Date: Friday, December 19, 2008	Sheet 7 of 61	


ANB1A
PART 1 OF 6
HYPER TRANSPORT CPU I/F
HT_RXCAD0P HT_RXCAD0N HT_RXCAD1P HT_RXCAD1N HT_RXCAD2P HT_RXCAD2N HT_RXCAD3P HT_RXCAD3N HT_RXCAD4P HT_RXCAD4N HT_RXCAD5P HT_RXCAD5N HT_RXCAD6P HT_RXCAD6N HT_RXCAD7P HT_RXCAD7N
HT_RXCAD8P HT_RXCAD8N HT_RXCAD9P HT_RXCAD9N HT_RXCAD10P HT_RXCAD10N HT_RXCAD11P HT_RXCAD11N HT_RXCAD12P HT_RXCAD12N HT_RXCAD13P HT_RXCAD13N HT_RXCAD14P HT_RXCAD14N HT_RXCAD15P HT_RXCAD15N
HT_RXCLK0P HT_RXCLK0N HT_RXCLK1P HT_RXCLK1N
HT_RXCTL0P HT_RXCTL0N HT_RXCTL1P HT_RXCTL1N
HT_RXCALP HT_RXCALN
HT_TXCAD0P HT_TXCAD0N HT_TXCAD1P HT_TXCAD1N HT_TXCAD2P HT_TXCAD2N HT_TXCAD3P HT_TXCAD3N HT_TXCAD4P HT_TXCAD4N HT_TXCAD5P HT_TXCAD5N HT_TXCAD6P HT_TXCAD6N HT_TXCAD7P HT_TXCAD7N
HT_TXCAD8P HT_TXCAD8N HT_TXCAD9P HT_TXCAD9N HT_TXCAD10P HT_TXCAD10N HT_TXCAD11P HT_TXCAD11N HT_TXCAD12P HT_TXCAD12N HT_TXCAD13P HT_TXCAD13N HT_TXCAD14P HT_TXCAD14N HT_TXCAD15P HT_TXCAD15N
HT_TXCLK0P HT_TXCLK0N HT_TXCLK1P HT_TXCLK1N
HT_TXCTL0P HT_TXCTL0N HT_TXCTL1P HT_TXCTL1N
HT_TXCALP HT_TXCALN
HT_NB_CPU_CAD_H0 HT_NB_CPU_CAD_L0 HT_NB_CPU_CAD_H1 HT_NB_CPU_CAD_L1 HT_NB_CPU_CAD_H2 HT_NB_CPU_CAD_L2 HT_NB_CPU_CAD_H3 HT_NB_CPU_CAD_L3 HT_NB_CPU_CAD_H4 HT_NB_CPU_CAD_L4 HT_NB_CPU_CAD_H5 HT_NB_CPU_CAD_L5 HT_NB_CPU_CAD_H6 HT_NB_CPU_CAD_L6 HT_NB_CPU_CAD_H7 HT_NB_CPU_CAD_L7
HT_NB_CPU_CAD_H8 HT_NB_CPU_CAD_L8 HT_NB_CPU_CAD_H9 HT_NB_CPU_CAD_L9 HT_NB_CPU_CAD_H10 HT_NB_CPU_CAD_L10 HT_NB_CPU_CAD_H11 HT_NB_CPU_CAD_L11 HT_NB_CPU_CAD_H12 HT_NB_CPU_CAD_L12 HT_NB_CPU_CAD_H13 HT_NB_CPU_CAD_L13 HT_NB_CPU_CAD_H14 HT_NB_CPU_CAD_L14 HT_NB_CPU_CAD_H15 HT_NB_CPU_CAD_L15
HT_NB_CPU_CLK_H0 HT_NB_CPU_CLK_L0 HT_NB_CPU_CLK_H1 HT_NB_CPU_CLK_L1
HT_NB_CPU_CTL_H0 HT_NB_CPU_CTL_L0 HT_NB_CPU_CTL_H1 HT_NB_CPU_CTL_L1
R344 301R2F-GP
R343 301R2F-GP
Placement: close RS780
Place < 100mils from pin C23 and A24
Place < 100mils from pin B25 and B24
RS780M-GP-U2
ANB1B
PART 2 OF 6
PCIE I/F GFX
PCIE I/F GPP
PCIE I/F SB
GFX_RX0P GFX_RX0N GFX_RX1P GFX_RX1N GFX_RX2P GFX_RX2N GFX_RX3P GFX_RX3N GFX_RX4P GFX_RX4N GFX_RX5P GFX_RX5N GFX_RX6P GFX_RX6N GFX_RX7P GFX_RX7N GFX_RX8P GFX_RX8N GFX_RX9P GFX_RX9N GFX_RX10P GFX_RX10N GFX_RX11P GFX_RX11N GFX_RX12P GFX_RX12N GFX_RX13P GFX_RX13N GFX_RX14P GFX_RX14N GFX_RX15P GFX_RX15N
GFX_TX0P GFX_TX0N GFX_TX1P GFX_TX1N GFX_TX2P GFX_TX2N GFX_TX3P GFX_TX3N GFX_TX4P GFX_TX4N GFX_TX5P GFX_TX5N GFX_TX6P GFX_TX6N GFX_TX7P GFX_TX7N GFX_TX8P GFX_TX8N GFX_TX9P GFX_TX9N GFX_TX10P GFX_TX10N GFX_TX11P GFX_TX11N GFX_TX12P GFX_TX12N GFX_TX13P GFX_TX13N GFX_TX14P GFX_TX14N GFX_TX15P GFX_TX15N
PEG_RXP0 PEG_RXN0 PEG_RXP1 PEG_RXN1 PEG_RXP2 PEG_RXN2 PEG_RXP3 PEG_RXN3 PEG_RXP4 PEG_RXN4 PEG_RXP5 PEG_RXN5 PEG_RXP6 PEG_RXN6 PEG_RXP7 PEG_RXN7 PEG_RXP8 PEG_RXN8 PEG_RXP9 PEG_RXN9 PEG_RXP10 PEG_RXN10 PEG_RXP11 PEG_RXN11 PEG_RXP12 PEG_RXN12 PEG_RXP13 PEG_RXN13 PEG_RXP14 PEG_RXN14 PEG_RXP15 PEG_RXN15
PEG_TXP0 PEG_TXN0 PEG_TXP1 PEG_TXN1 PEG_TXP2 PEG_TXN2 PEG_TXP3 PEG_TXN3 PEG_TXP4 PEG_TXN4 PEG_TXP5 PEG_TXN5 PEG_TXP6 PEG_TXN6 PEG_TXP7 PEG_TXN7 PEG_TXP8 PEG_TXN8 PEG_TXP9 PEG_TXN9 PEG_TXP10 PEG_TXN10 PEG_TXP11 PEG_TXN11 PEG_TXP12 PEG_TXN12 PEG_TXP13 PEG_TXN13 PEG_TXP14 PEG_TXN14 PEG_TXP15 PEG_TXN15
53 PEG_RXN[15..0]
53 PEG_RXP[15..0]
PEG_TXP[15..0] 53
PEG_TXN[15..0] 53
SCD1U16V2KX-3GP
RS780M Display Port Support(muxed on GFX)
DP0 GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1 GFX_TX4,TX5,TX6,TX7,AUX1,HPD1
GTXP0 GTXN0 GTXP1 GTXN1 GTXP2 GTXN2 GTXP3 GTXN3
UMA
HDMI_DATA2+ HDMI_DATA2- HDMI_DATA1+ HDMI_DATA1- HDMI_DATA0+ HDMI_DATA0- HDMI_CLK+ HDMI_CLK-
2008/11/05 LAN
2008/11/05 MINICARD1
2008/11/05 MINICARD2
NEW CARD
PCIE_RXP1 PCIE_RXN1 PCIE_RXP2 PCIE_RXN2 PCIE_RXP3 PCIE_RXN3 PCIE_RXP5 PCIE_RXN5
PCIE_TXP1 PCIE_TXN1 PCIE_TXP2 PCIE_TXN2 PCIE_TXP3 PCIE_TXN3 PCIE_TXP5 PCIE_TXN5
TPAD14-GP
TP21 TP20 TP16 TP17
GPP_RX5P GPP_RX5N GPP_TX5P GPP_TX5N
A-LINK
11 ALINK_NBRX_SBTX_P0 ALINK_NBRX_SBTX_N0 ALINK_NBRX_SBTX_P1 ALINK_NBRX_SBTX_N1 ALINK_NBRX_SBTX_P2 ALINK_NBRX_SBTX_N2 ALINK_NBRX_SBTX_P3 ALINK_NBRX_SBTX_N3
ALINK_NBTX_C_SBRX_P0 ALINK_NBTX_C_SBRX_N0 ALINK_NBTX_C_SBRX_P1 ALINK_NBTX_C_SBRX_N1 ALINK_NBTX_C_SBRX_P2 ALINK_NBTX_C_SBRX_N2 ALINK_NBTX_C_SBRX_P3 ALINK_NBTX_C_SBRX_N3
PCE_PCAL PCE_NCAL
R315 R16 1K27R2F-L-GP 2KR2F-3-GP
1D1V_S0
Place < 100mils from pin AB8 and AB8
http://hobi-elektronika.net
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS780M_HT LINK&PCIe(1/3)
Size A3
Document Number
JV50-PU
Rev SB
Date: Friday, December 19, 2008
Sheet 8 of 61


STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable
RS780: Enables Side port memory (RS780 use HSYNC#)
*1 :Disable 0 : Enable
SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected
Close to NB ball
R69 BOM Option
ENABLE External CLK GEN
ANB1C
PART 3 OF 6
CRT/TVOUT
PWR
LVTM
PLL
PM
CLOCKs
MIS.
RS780M-GP-U2
GPIO MODE
STRP_DATA 0 *1
VCC_NB 1.1V 1.0V
http://hobi-elektronika.net
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS780M LVDS&CRT (2/3)
Size A3
Document Number JV50-PU
Rev SB
Date: Friday, December 19, 2008
Sheet 9 of 61


0.6A per ANT Rev1.1, Page3
0.45A per ANT Rev1.1, Page3
80mil Width
300mil Width
10A per ANT Rev1.1, Page3
Per check list (Rev 0.02)
RS780M: 1V ~ 1.1V, check PWR team
+NB_VCORE
POWER
PART 5/6
ANB1E
RS780M-GP-U2
GROUND
PART 6/6
ANB1F
SBD_MEM/DVO_I/F
PAR 4 OF 6
ANB1D
MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions
http://hobi-elektronika.net
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-RS780M Side Port&PWR&GND(3/3)
JV50-PU
Friday, December 19, 2008


ASB1A
SB700
Part 1 of 5
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
RTC
CPU
SB700-1-GP-U1
R146 33R2J-2-GP
NB_RST#
9,26,33,36 PLT_RST1#
A_RST#
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
PCIE_CALRP
PCIE_CALRN
PCIE_PVDD
PCIE_PVSS
R143 562R2F-GP PCIE_CALRP
R147 2K05R2F-GP PCIE_CALRN
1D2V_S0
+1.2V_RUN_PCIE_PVDD
PCIE_VDDR
L24 PBY201209T-221Y-N-GP
220 ohm 2A
2ND = 68.00216.161
>15mil Width
43 mA
C810 SC1U10V2KX-1GP
C811 SC1U10V2KX-1GP
Place R <100mils form pins T25,T24
3D3V_S5
U16A
TSLVC08APW-1-GP
73.07408.L16
2ND = 73.07408.L15
3RD = 73.07408.02B
PLT_RST1#_B 32,33,34,37,53
CLK_PCIE_SB
CLK_PCIE_SB#
PCIE_RCLKP/NB_LNK_CLKP
PCIE_RCLKN/NB_LNK_CLKN
NB_DISP_CLKP
NB_DISP_CLKN
NB_HT_CLKP
NB_HT_CLKN
CPU_HT_CLKP
CPU_HT_CLKN
SLT_GFX_CLKP
SLT_GFX_CLKN
GPP_CLK0P
GPP_CLK0N
GPP_CLK1P
GPP_CLK1N
GPP_CLK2P
GPP_CLK2N
GPP_CLK3P
GPP_CLK3N
CLK_SB_25M
CLK_SB_25M_1
25M_48M_66M_OSC
25M_X1
25M_X2
X1
X2
For SB710
2008/11/06
DY
R162 10MR2J-L-GP
C424 SC15P50V2JN-2-GP
32K_X1
X-32D768KHZ-38GPU X4
R164 10MR2J-L-GP
82.30001.691
2ND = 82.30001.861
C433 SC15P50V2JN-2-GP
32K_X2
R440 0R2J-2-GP
TP209 TPAD14-GP
TP210 TPAD14-GP
2008/11/06
NB_ALLOW_LDTSTOP
PROCHOT#_SB
CPU_PWRGD
CPU_LDT_STOP#
CPU_LDT_RST#
ALLOW_LDTSTP
PROCHOT#
LDT_PG
LDT_STP#
LDT_RST#
PCICLK0
PCICLK1
PCICLK2
PCICLK3
PCICLK4
PCICLK5/GPIO41
PCI_CLK0_R
PCI_CLK1_R
PCI_CLK2_R
PCI_CLK3_R
PCI_CLK4_R
PCI_CLK5_R
R144 0R0402-PAD
R141 0R0402-PAD
R137 0R0402-PAD
R138 0R0402-PAD
TP204 TPAD14-GP
TP203 TPAD14-GP
PCI_CLK2 15
PCI_CLK3 15
CLK_PCI4 15
CLK_PCI_LOM 15
EC42 EC41 EC39 EC40
SC22P50V2JN-4GP
PCIRST#
PCIRST#_SB
TP138 TPAD14-GP
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31
CBE0# CBE1# CBE2# CBE3#
FRAME# DEVSEL# IRDY# TRDY# PAR STOP# PERR# SERR#
REQ0# REQ1# REQ2# REQ3#/GPIO70 REQ4#/GPIO71
GNT0# GNT1# GNT2# GNT3#/GPIO72 GNT4#/GPIO73
CLKRUN# LOCK#
PCI_AD23 15
PCI_AD24 15
PCI_AD25 15
PCI_AD26 15
PCI_AD27 15
PCI_AD28 15
PCI_AD29 15
PCI_AD30 15
PCI_REQ#0
PCI_REQ#1
PCI_REQ#2
PCI_REQ#3
PCI_REQ#4
PCI_GNT#0
PCI_GNT#1
PCI_GNT#2
PCI_GNT#3
PCI_GNT#4
PCI_LOCK#
TP124 TPAD14-GP
TP119 TPAD14-GP
TP198 TPAD14-GP
TP115 TPAD14-GP
TP197 TPAD14-GP
TP117 TPAD14-GP
TP121 TPAD14-GP
TP118 TPAD14-GP
TP192 TPAD14-GP
TP120 TPAD14-GP
TP201 TPAD14-GP
PM_CLKRUN# 36
R126 10KR2J-3-GP
INTE#/GPIO33
INTF#/GPIO34
INTG#/GPIO35
INTH#/GPIO36
INT_PIRQE#
INT_PIRQF#
INT_PIRQG#
INT_PIRQH#
TP116 TPAD14-GP
TP191 TPAD14-GP
TP123 TPAD14-GP
TP122 TPAD14-GP
LPC_LAD[0..3]
LPC_LAD[0..3] 36,37
RN51 SRN22-3-GP
LPCCLK0
LPCCLK1
LAD0
LAD1
LAD2
LAD3
LFRAME#
LDRQ0#
LDRQ1#/GNT5#/GPIO68
BMREQ#/REQ5#/GPIO65
SERIRQ
LPCCLK0_R
LPCCLK1_R
LPC_LFRAME# 36,37
PCLK_FWH 15,37
PCLK_KBC 15,36
EC48 EC47
SC22P50V2JN-4GP
INT_SERIRQ 36
PCI_REQ#5 12
TP213 TPAD14-GP
TP193 TPAD14-GP
RTCCLK
INTRUDER_ALERT#
VBAT
RTC_CLK 15,35
INTRUDER#
RTC_AUX_S5_R
TP148 TPAD14-GP
R158 1KR2J-1-GP
RTC_AUX_S5
C407 SC1U10V2KX-1GP
C408 SCD1U16V2ZY-2GP
C409 SCD1U16V2ZY-2GP
ARTC1
PWR
GND
NP1
NP2
BAT-CON2-1-GP-U
62.70001.011
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB700 PCIE&PCI (1/5)
Size A3
Document Number JV50-PU
Rev SB
Date: Friday, December 19, 2008
Sheet 11 of 61
http://hobi-elektronika.net



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700 USB&GPIO (2/5)

Size: A3 | Document Number: JV50-PU | Rev: SB

Date: Friday, December 19, 2008 | Sheet 12 of 61

PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB700

SATA HDD
SATA ODD

SB700
Part 2 of 5

SERIAL ATA
ATA 66/100/133
SPI ROM
SATA PWR
HW MONITOR

2008/11/06
2008/12/11
Very Close to SB700

82.30020.A31
2ND = 82.30020.851

Dummy CKG select

CLK_ID
(1,0)
ICS: 0,0
SEG: 0,1
RTM: 1,0

Layout connect to Cap then GND

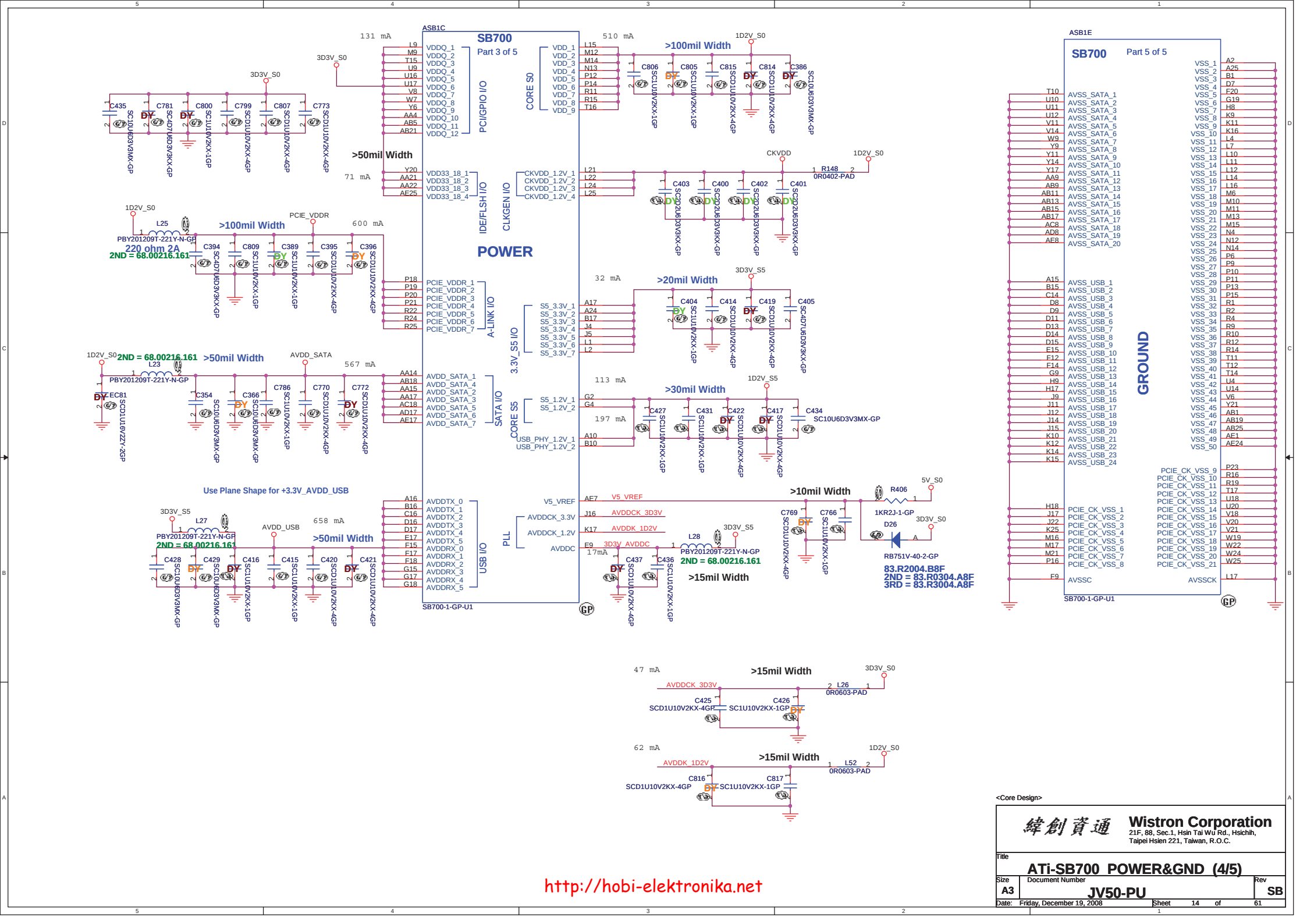
SB700-1-GP-U1

http://hobi-elektronika.net

<Core Design>

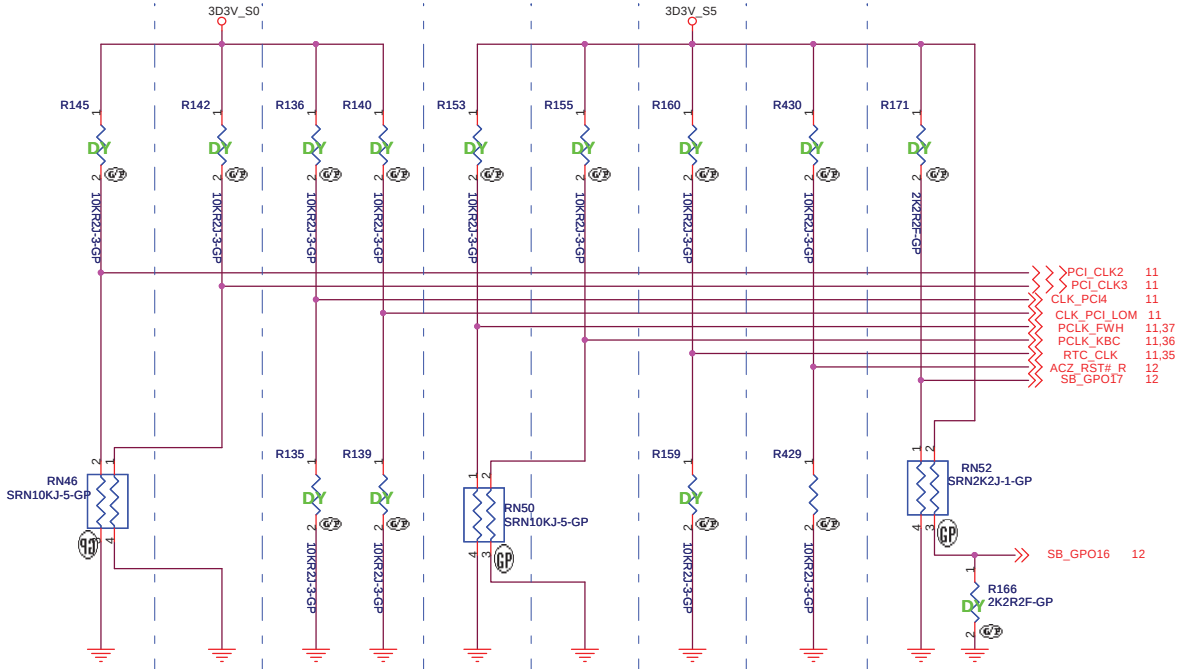
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700 SATA-IDE (3/5)
Size: A3
Document Number: JV50-PU
Rev: SB
Date: Friday, December 19, 2008
Sheet 13 of 61


ASB1C
SB700
Part 3 of 5
POWER
131 mA
>50mil Width
71 mA
510 mA
>100mil Width
1D2V_S0
3D3V_S0
CKVDD
R148
0R0402-PAD
PCIE_VDDR
600 mA
L25
PBY201209T-221Y-N-GP
220 ohm 2A
2ND = 68.00216.161
32 mA
>20mil Width
3D3V_S5
113 mA
>30mil Width
1D2V_S5
197 mA
AVDD_SATA
567 mA
L23
>50mil Width
Use Plane Shape for +3.3V_AVDD_USB
3D3V_S5
L27
AVDD_USB
658 mA
>10mil Width
5V_S0
R406
1KR2J-1-GP
D26
RB751V-40-2-GP
83.R2004.B8F
2ND = 83.R0304.A8F
3RD = 83.R3004.A8F
L28
>15mil Width
17mA
PCI/GPIO I/O
CORE S0
IDE/FLSH I/O
CLKGEN I/O
A-LINK I/O
3.3V_S5 I/O
SATA I/O
CORE S5
USB I/O
PLL
SB700-1-GP-U1
ASB1E
SB700
Part 5 of 5
GROUND
SB700-1-GP-U1
47 mA
>15mil Width
L26
0R0603-PAD
62 mA
>15mil Width
L52
0R0603-PAD
http://hobi-elektronika.net
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB700 POWER&GND (4/5)
Size
A3
Document Number
JV50-PU
Rev
SB
Date: Friday, December 19, 2008
Sheet 14 of 61

REQUIRED STRAPS

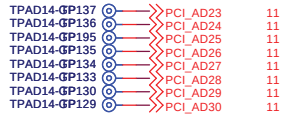
REQUIRED SYSTEM STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved; H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM; L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

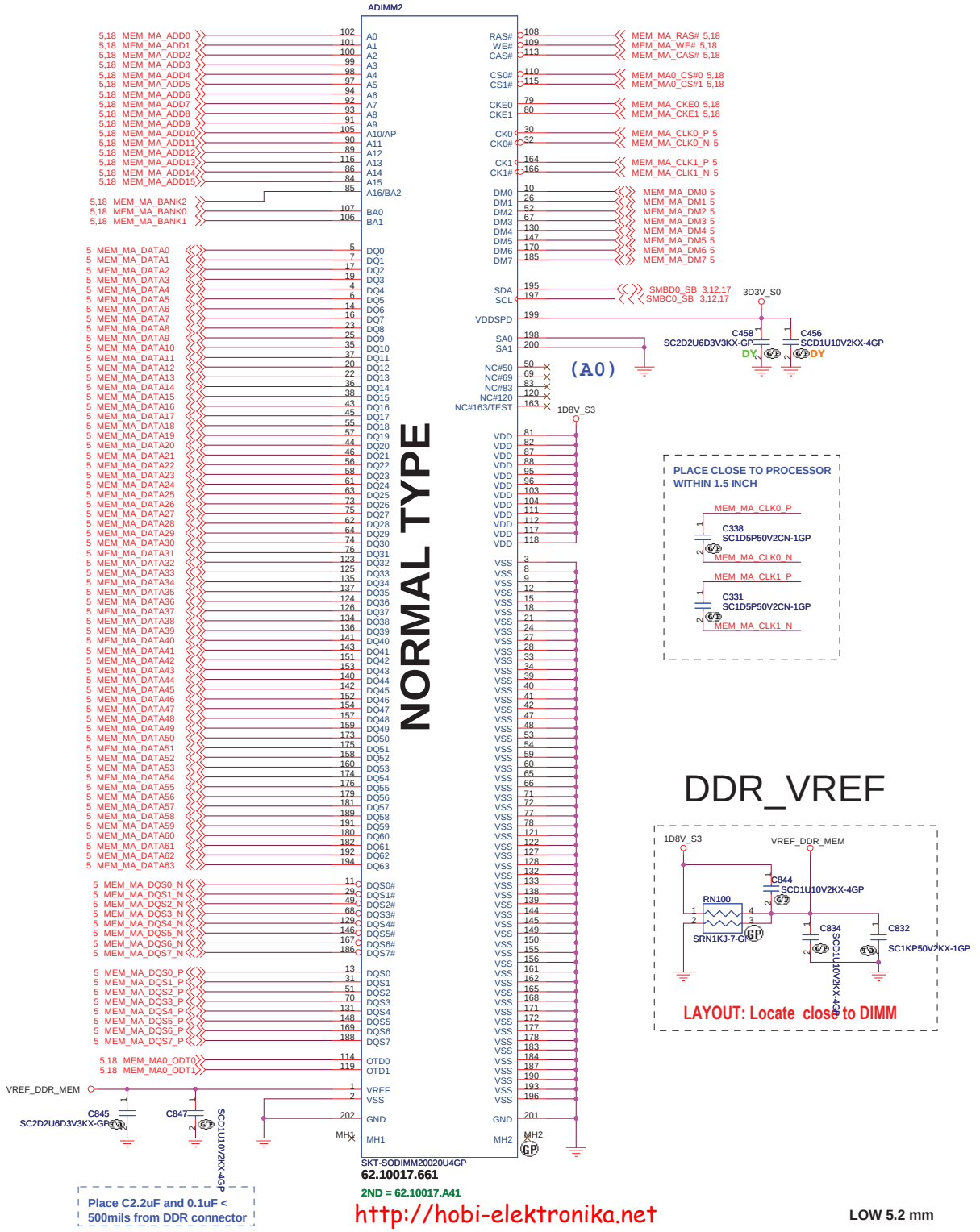
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700 STRAPPING (5/5)

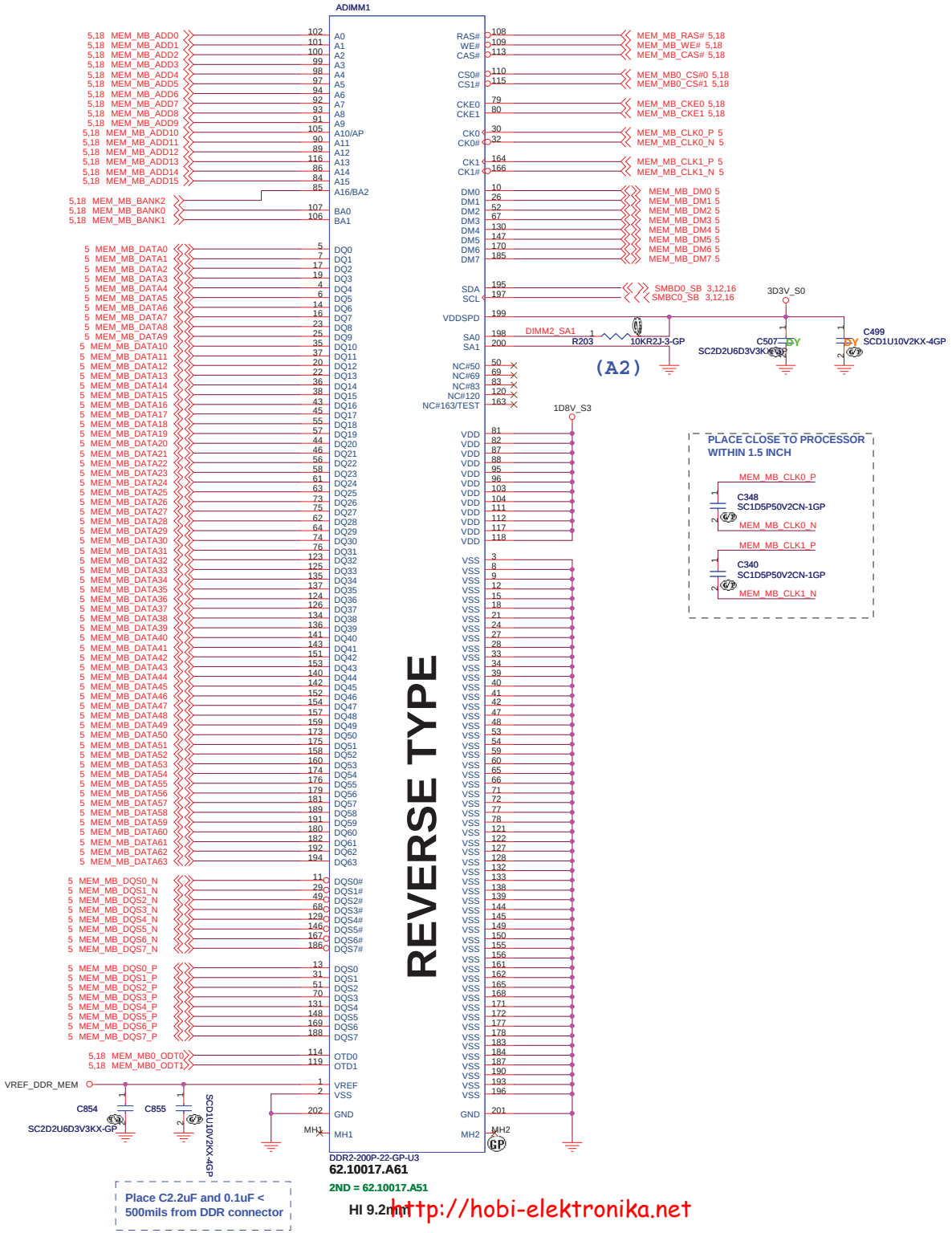
Size: A3 | Document Number: JV50-PU | Rev: SB

Date: Friday, December 19, 2008 | Sheet 15 of 61



<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DDR_SO-DIMM SKT_1	
Size: Custom	Document Number: JV50-PU	Rev: SB
Date: Friday, December 19, 2008	Sheet 16 of 61	



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

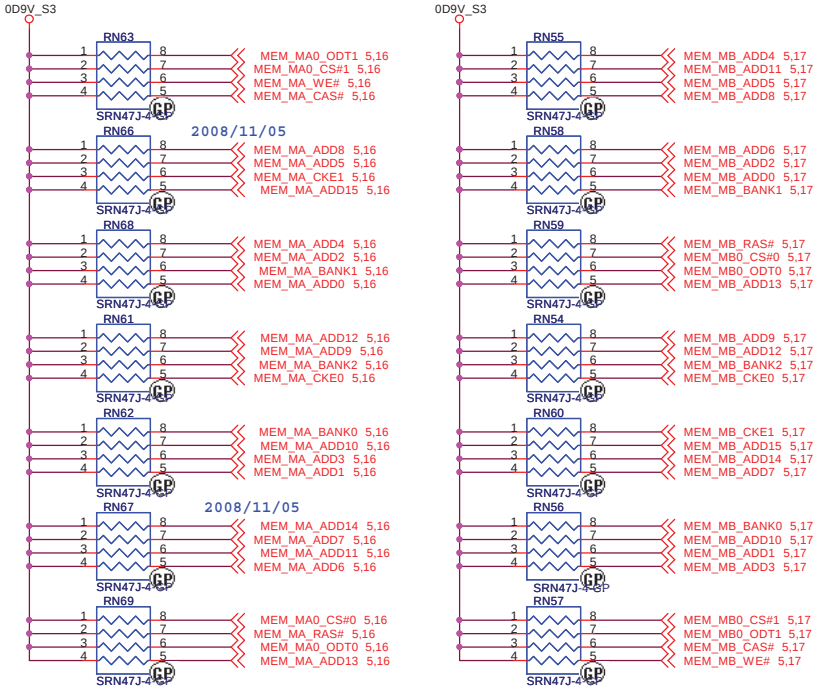
Title: DDR_SO-DIMM SKT_2

Size: Custom | Document Number: JV50-PU | Rev: SB

Date: Friday, December 19, 2008 | Sheet 17 of 61

PARALLEL TERMINATION

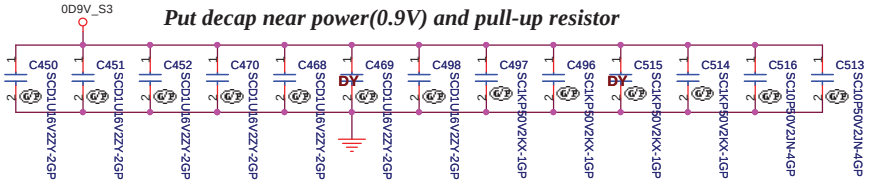
Put decap near power(0.9V) and pull-up resistor



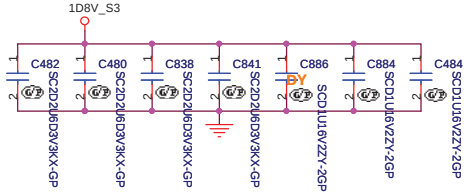
Do not share the Term resistor between the DDR addess and Control Signals.

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

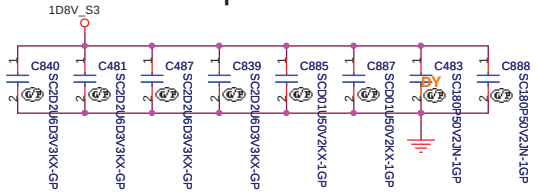


Place these Caps near DM1



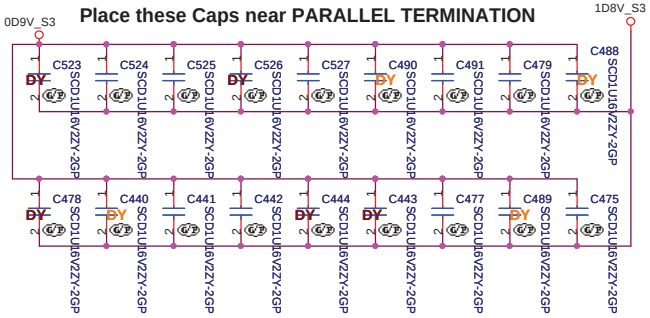
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION



<Core Design>

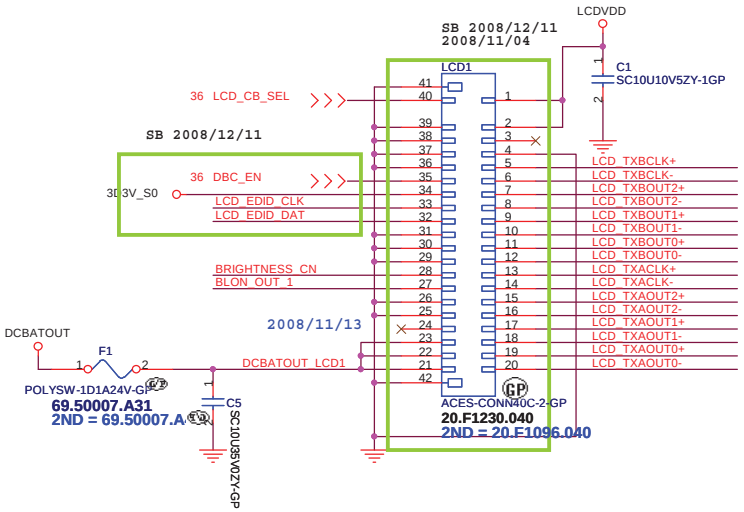
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

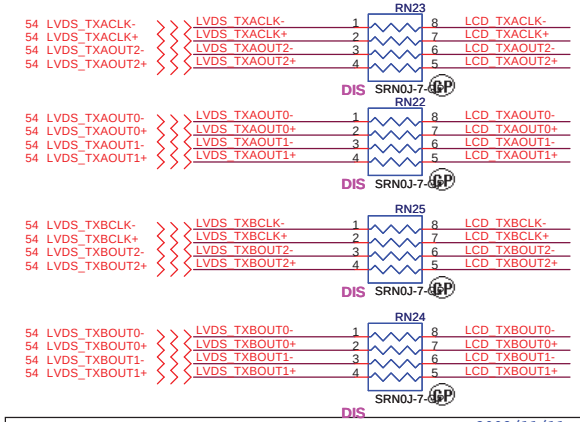
Title: **DDR_DAMPING & TERMINATION**

Size	Document Number	Rev
A3	JV50-PU	SB

Date: Friday, December 19, 2008 Sheet 18 of 61

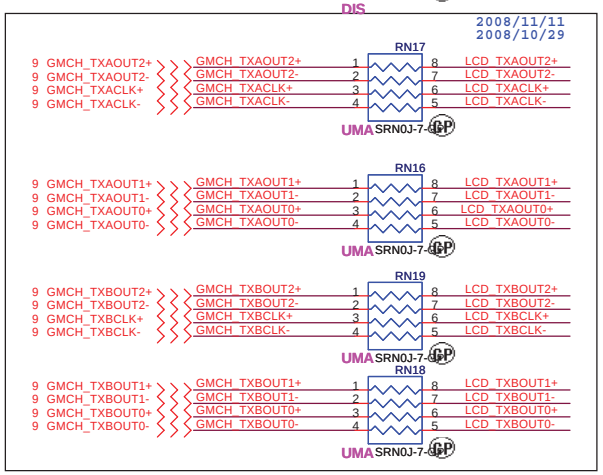
LCD/INVERTER/CCD CONN



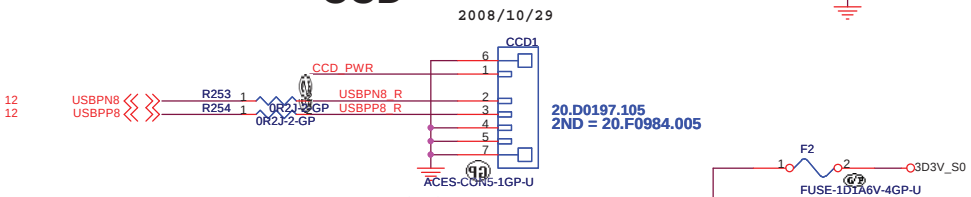


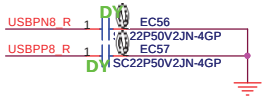
Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

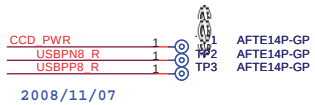
CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

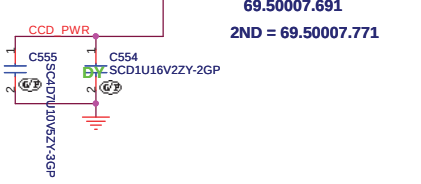


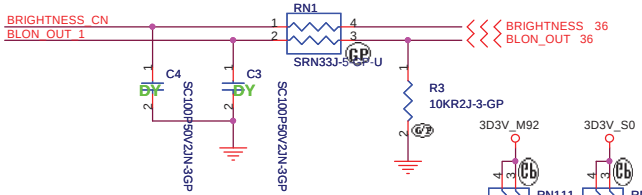
CCD

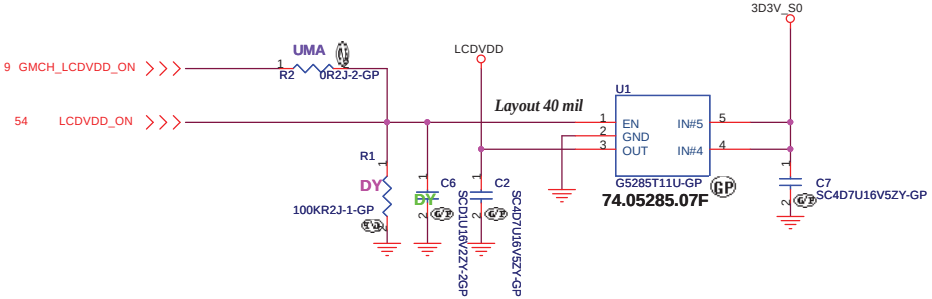


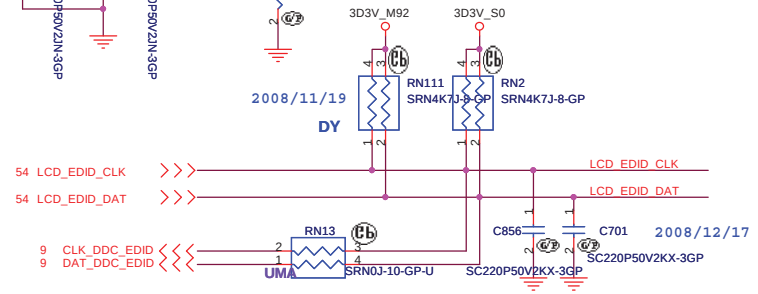












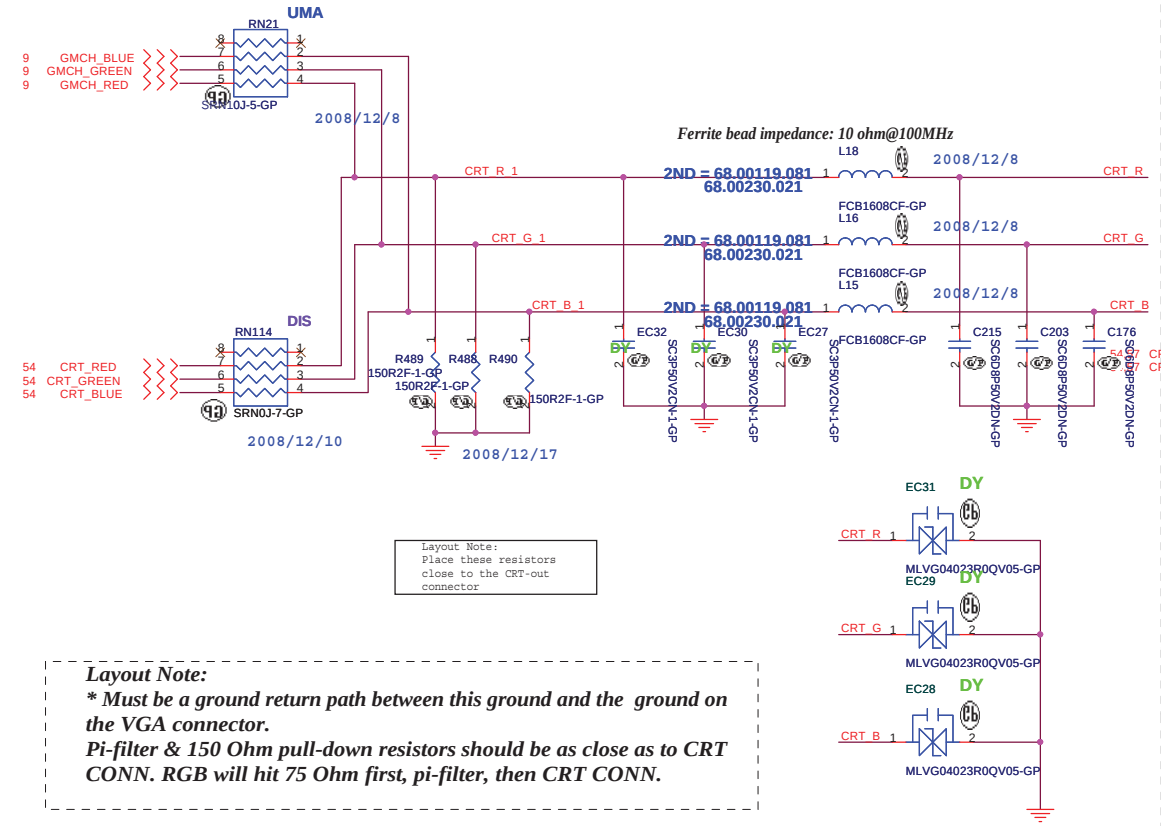
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

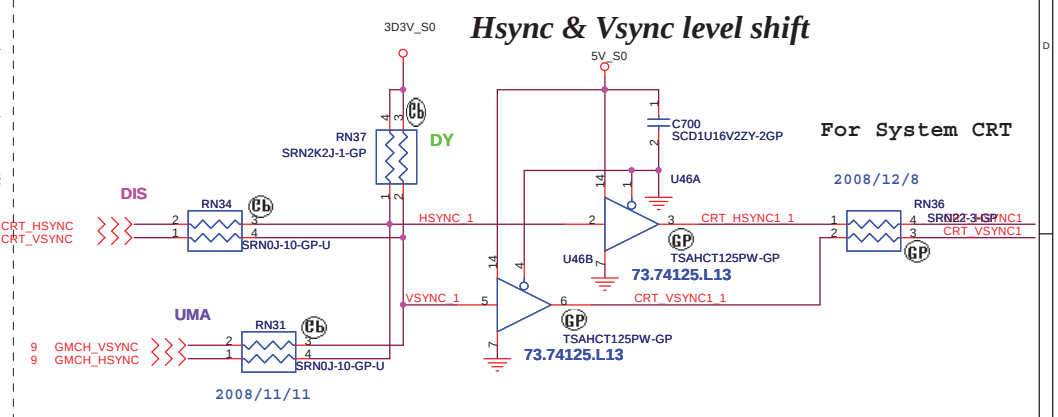
Title: LCD CONN

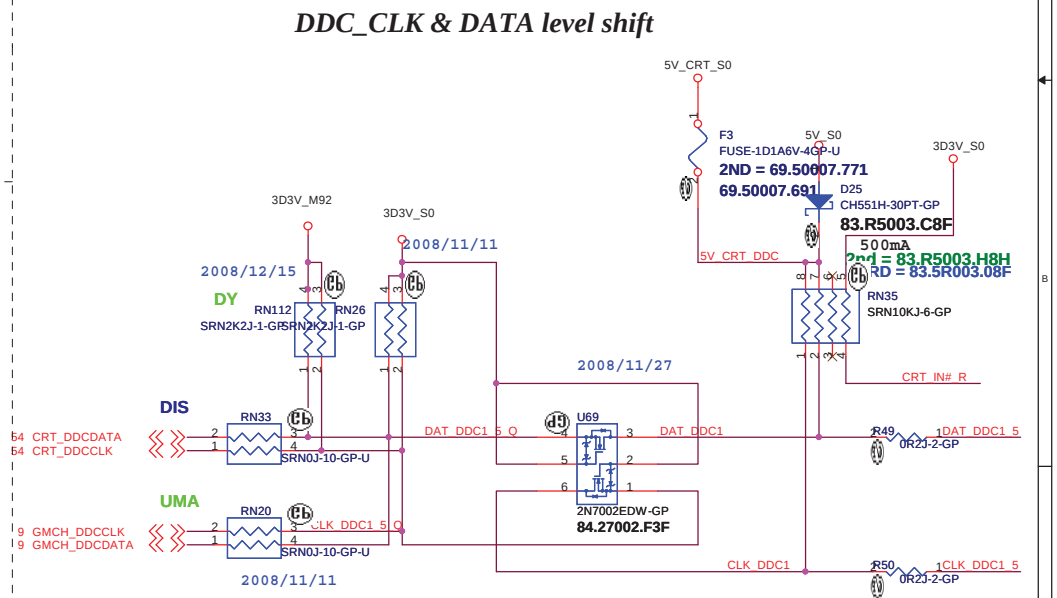
Size: A3 | Document Number: JV50-PU | Rev: SB

Date: Friday, December 19, 2008 | Sheet 19 of 61

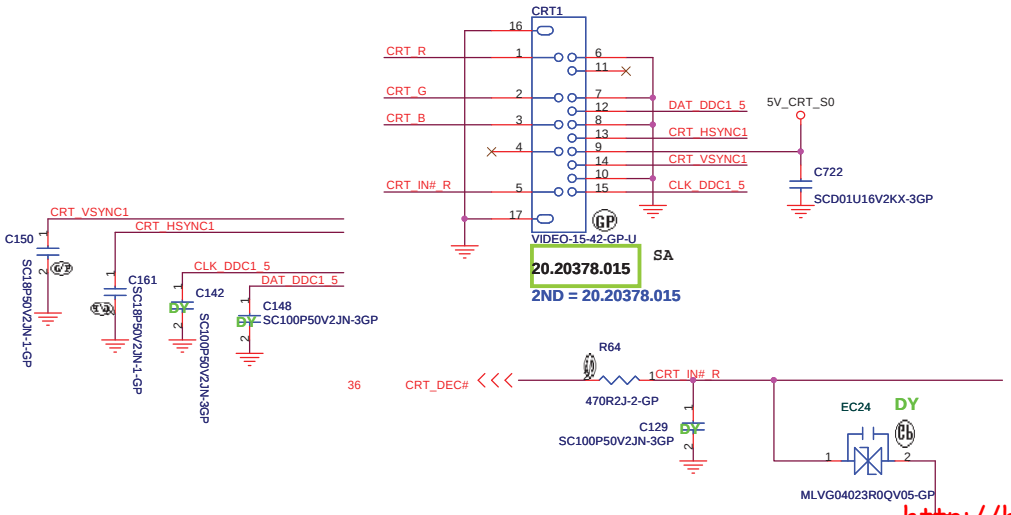


Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.





CRT I/F & CONNECTOR



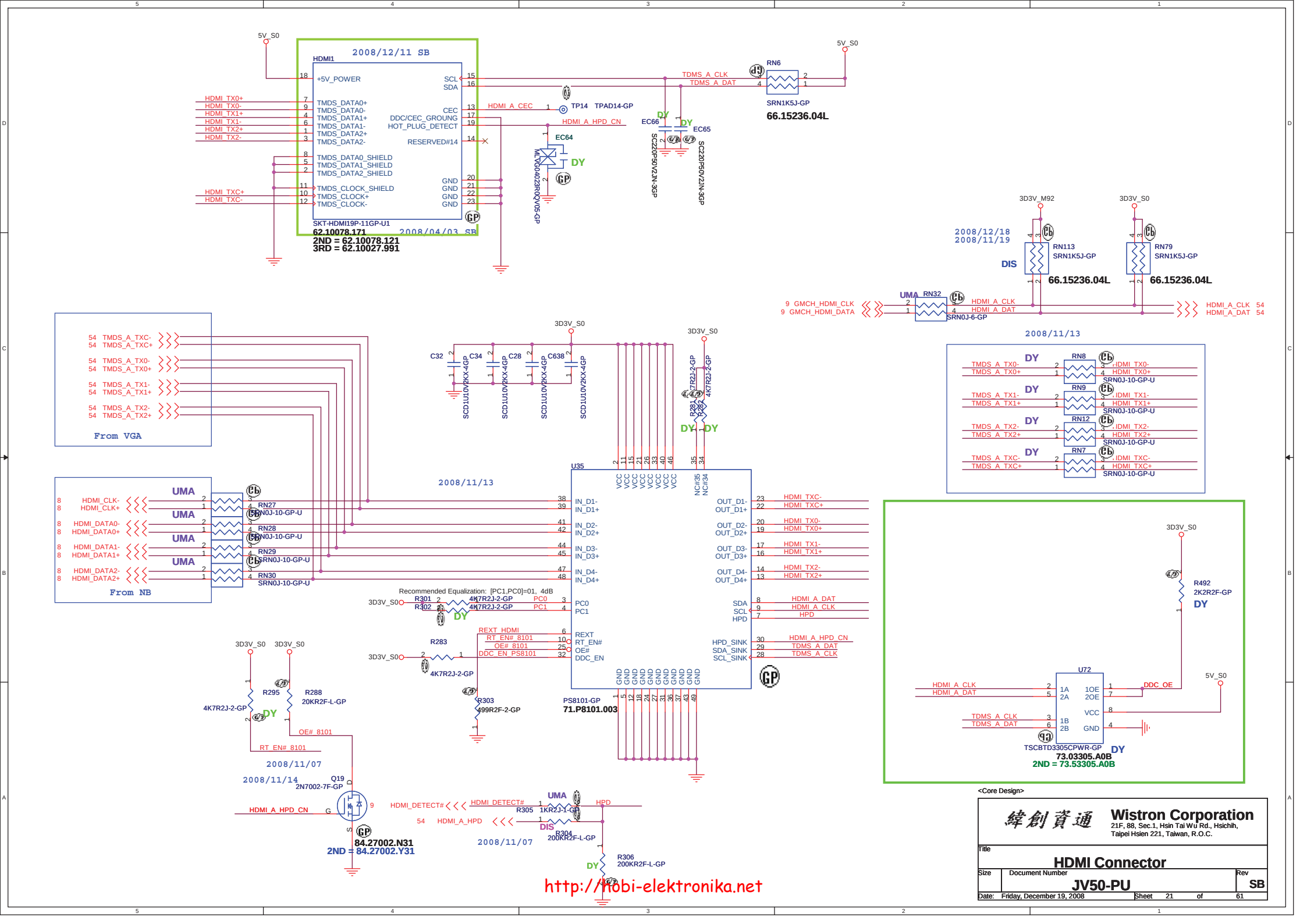
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

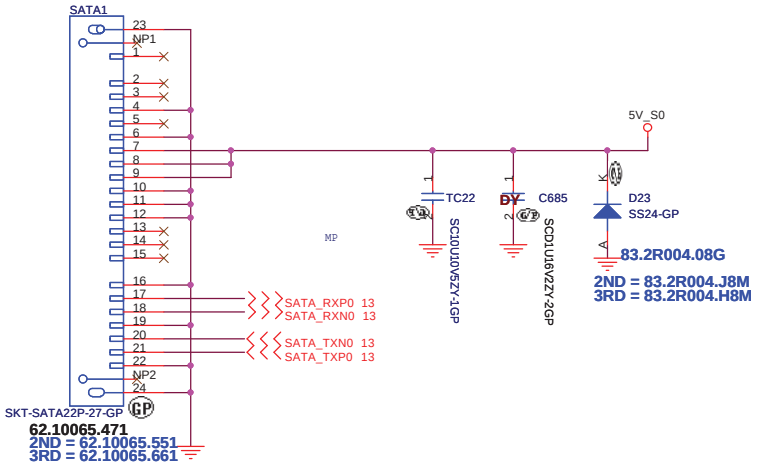
Title: **CRT Connector**

Size	Document Number	Rev
	JV50-PU	SB

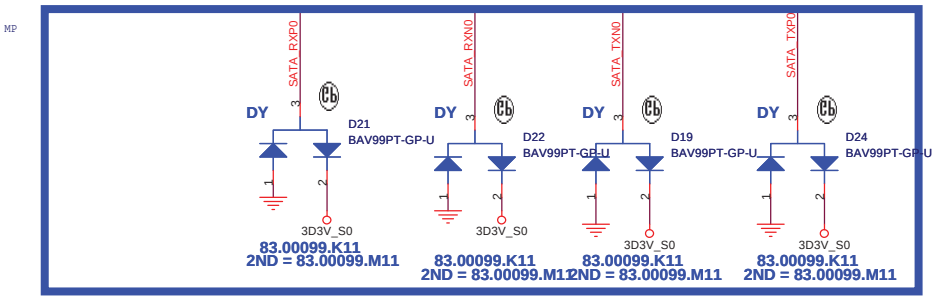
Date: Friday, December 19, 2008 Sheet 20 of 61


2008/12/11 SB
HDMI1
SKT-HDMI19P-11GP-U1
62.10078.171
2008/04/03 SB
2ND = 62.10078.121
3RD = 62.10027.991
RN6
SRN1K5J-GP
66.15236.04L
TP14 TPAD14-GP
EC64
EC65
EC66
DY
2008/12/18
2008/11/19
DIS
RN113
RN79
3D3V_M92
3D3V_S0
UMA RN32
SRN0J-6-GP
2008/11/13
From VGA
From NB
U35
PS8101-GP
71.P8101.003
Recommended Equalization: [PC1,PC0]=01, 4dB
R492
2K2R2F-GP
U72
TSCBTD3305CPWR-GP
73.03305.A0B
2ND = 73.53305.A0B
Q19
2N7002-7F-GP
84.27002.N31
2ND = 84.27002.Y31
2008/11/07
2008/11/14
http://hobi-elektronika.net
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
HDMI Connector
Size
Document Number
JV50-PU
Rev
SB
Date: Friday, December 19, 2008
Sheet 21 of 61

SATA Connector



2008/12/17



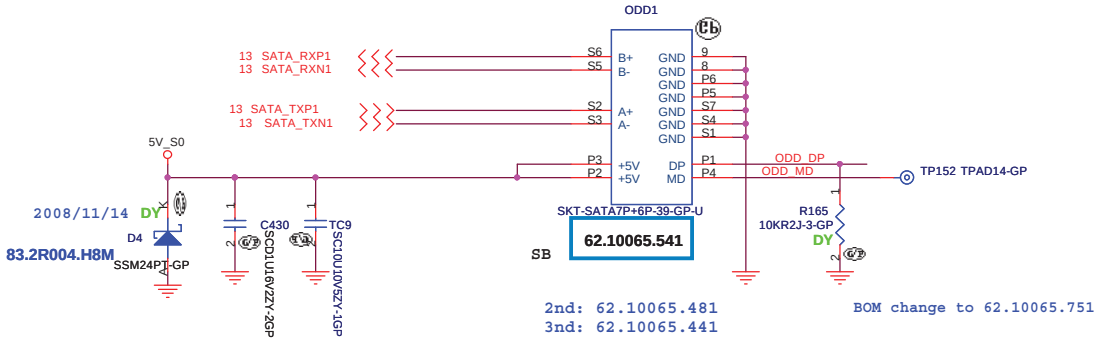
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

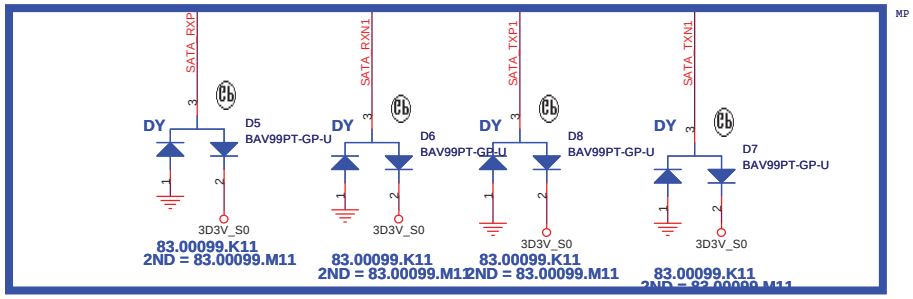
Title		
HDD		
Size	Document Number	Rev
	JV50-PU	SB
Date: Friday, December 19, 2008	Sheet 22 of 61	

SATA ODD Connector

2008/11/12



2008/12/17



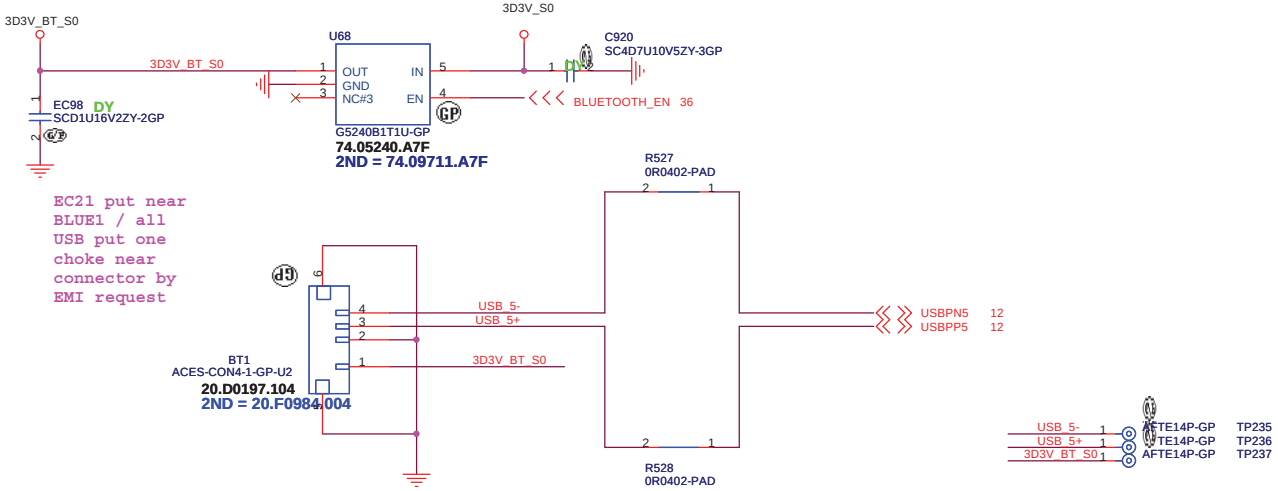
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

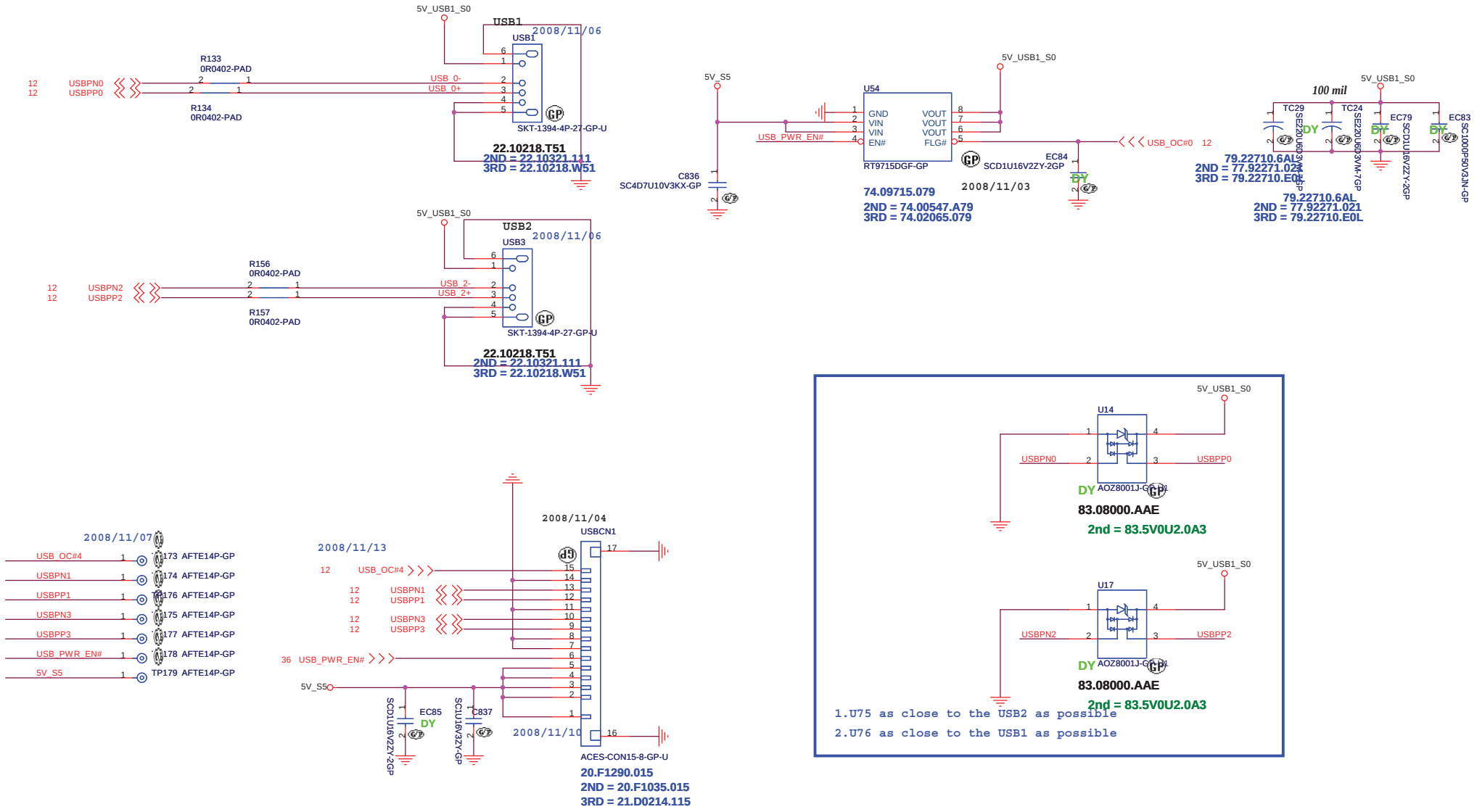
Title	ODD	
Size	Document Number JV50-PU	Rev SB
Date: Friday, December 19, 2008	Sheet 23 of 61	

BLUETOOTH MODULE

1.5A / High Active Voltage 2V



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	BLUETOOTH	
Size	Document Number JV50-PU	Rev SB
Date: Friday, December 19, 2008	Sheet 24 of 61	



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**USB**
Size	Document Number: **JV50-PU** Rev: **SB**
Date: Friday, December 19, 2008	Sheet 25 of 61

CO-Layout BCM5764 and BCM5784
modify BOM :71.05784.003

2008/10/28

U4

BCM5764MKMLG-GP
71.05764.M01
2ND = 71.05784.003

U3
AT45DB011D-SH-T-GP
72.45011.B01

Q5
BCP69-GP
84.00069.B1B
2ND = 84.DCP69.01B
3RD = 84.00069.A1B

X1
XTAL-25MHZ-120-GP-U
82.30020.A31
2ND = 82.30020.B61

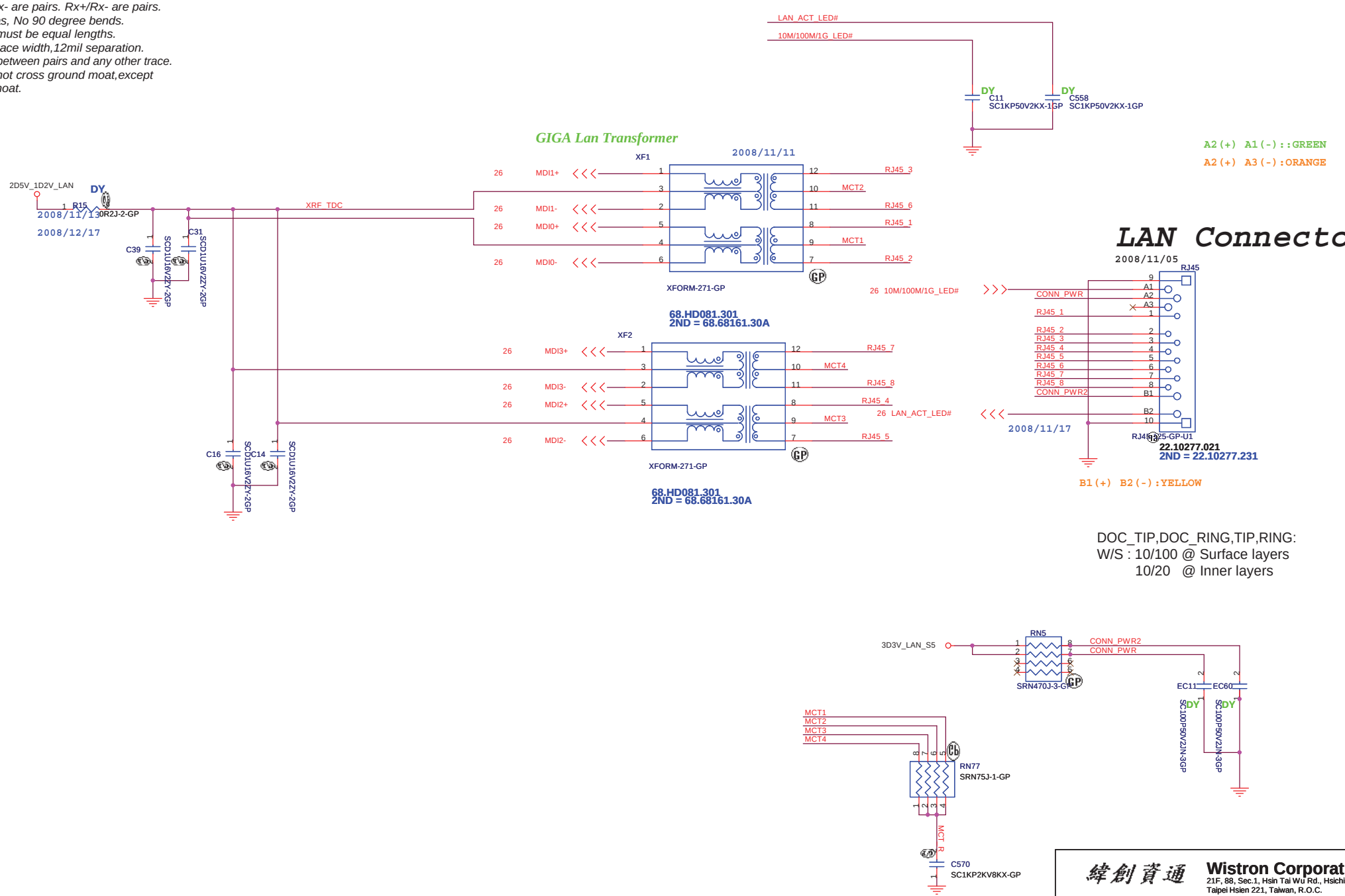
2008/11/13

Place PLLVDD/AVDDL
CKT as close to chip as
possible

緯創資通	Wistron Corporation
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	BCM5764MKMLG
Size A3	Document Number JV50-PU Rev SB
Date: Friday, December 19, 2008	Sheet 26 of 61

LAN Connector

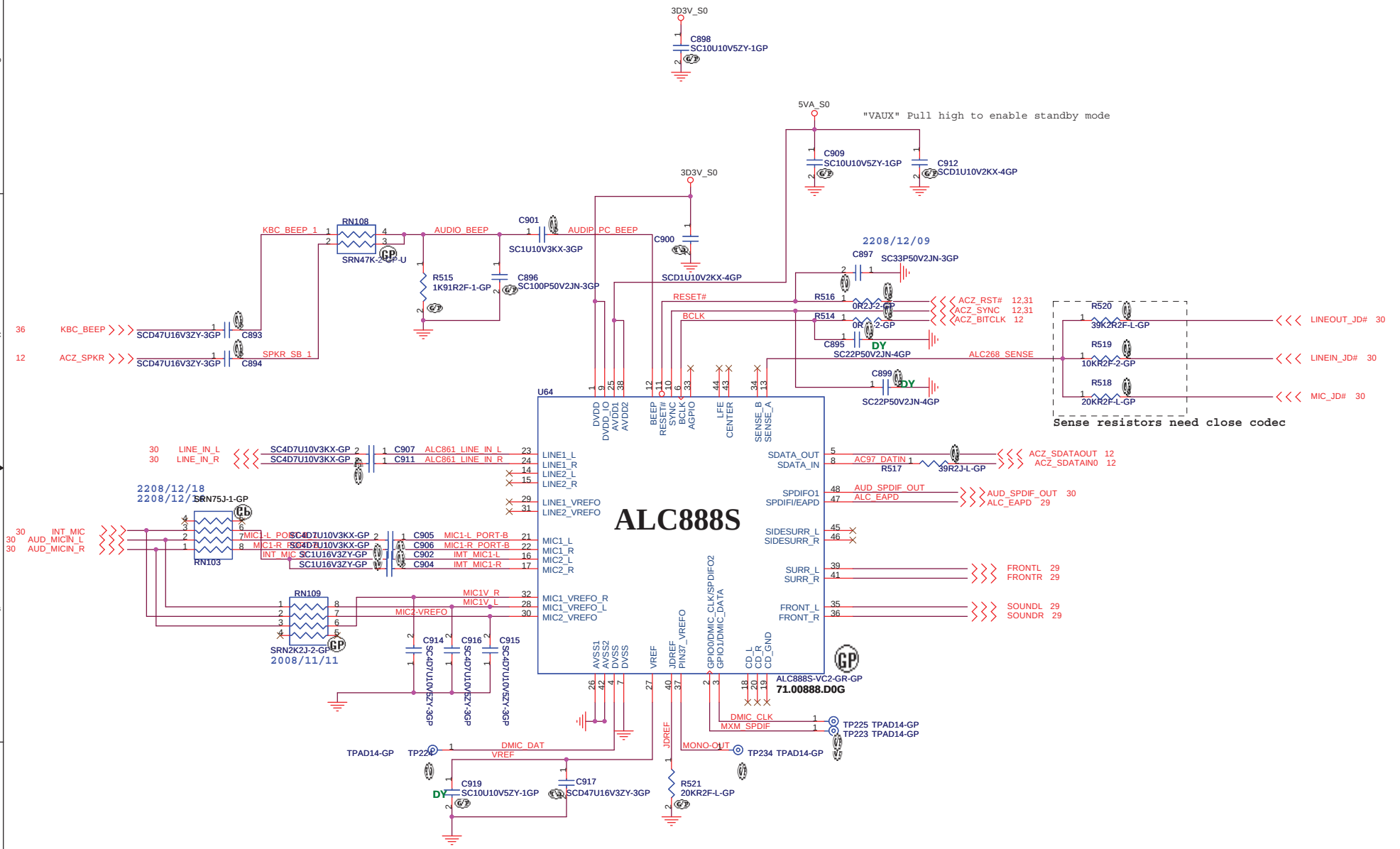
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.



http://hobi-elektronika.net

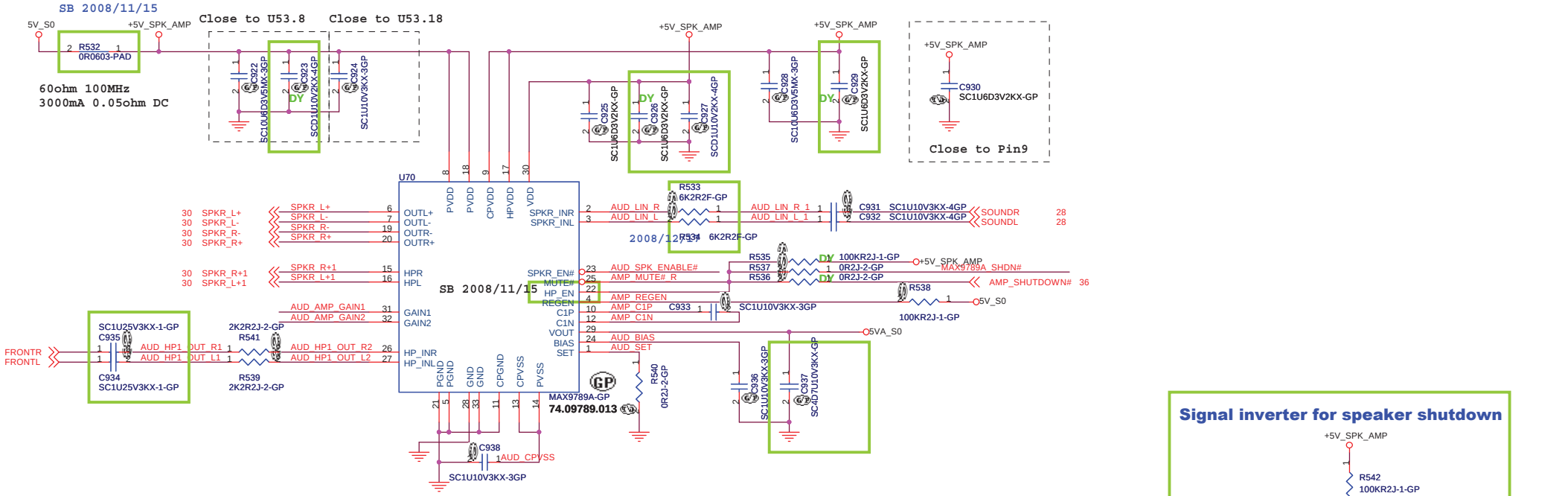
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

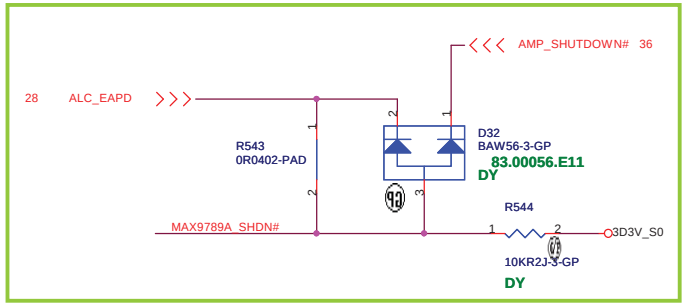
Title: LAN CONN		
Size: A3	Document Number: JV50-PU	Rev: SB
Date: Friday, December 19, 2008	Sheet 27 of 61	



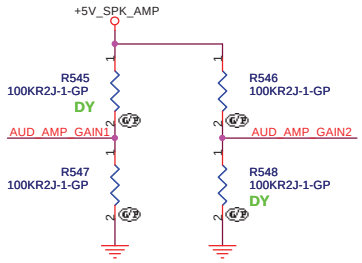
http://hobi-elektronika.net

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Azalia codec ALC888	
Size A3	Document Number JV50-PU	Rev SB
Date: Friday, December 19, 2008	Sheet 28 of 61	



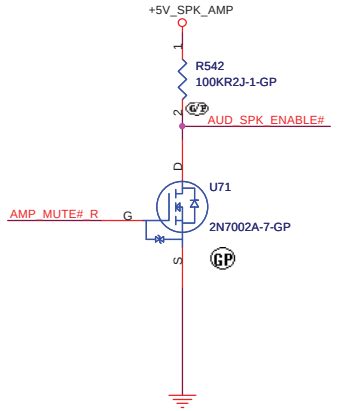


GAIN SETTING



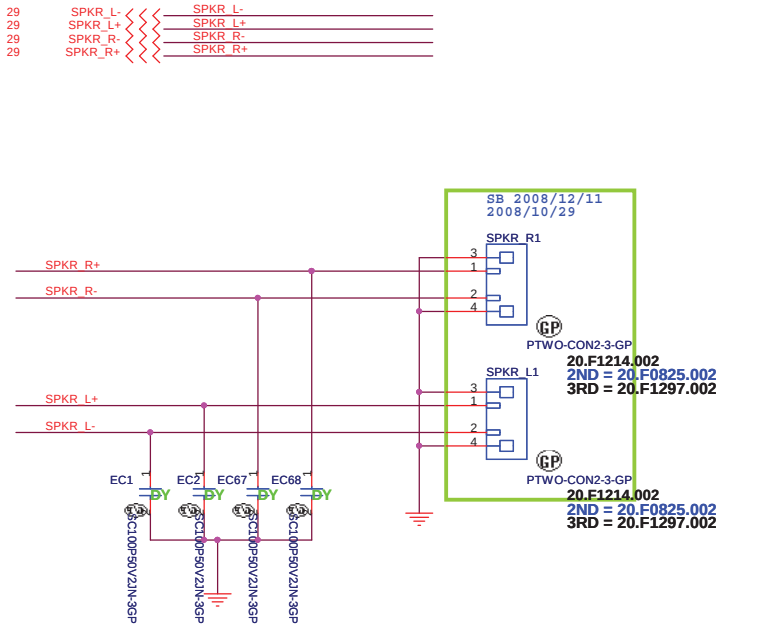
GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

Signal inverter for speaker shutdown

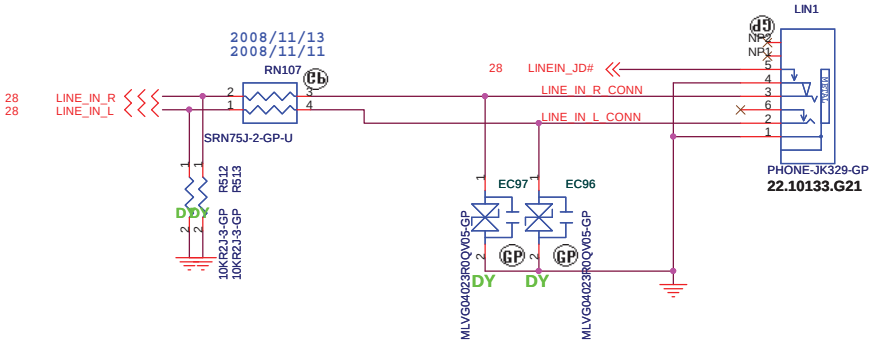


緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	AUDIO AMP
Size	Document Number: JV50-PU
Rev	SB
Date: Friday, December 19, 2008	Sheet 29 of 61

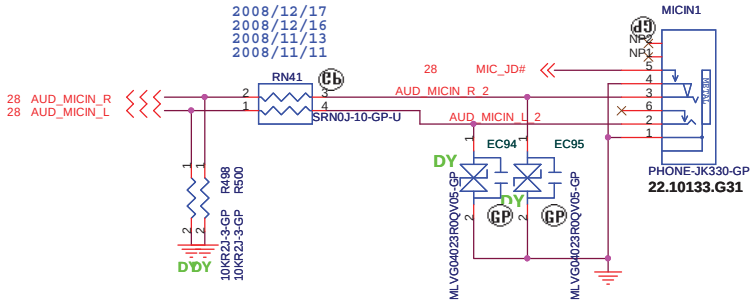
Internal Speaker



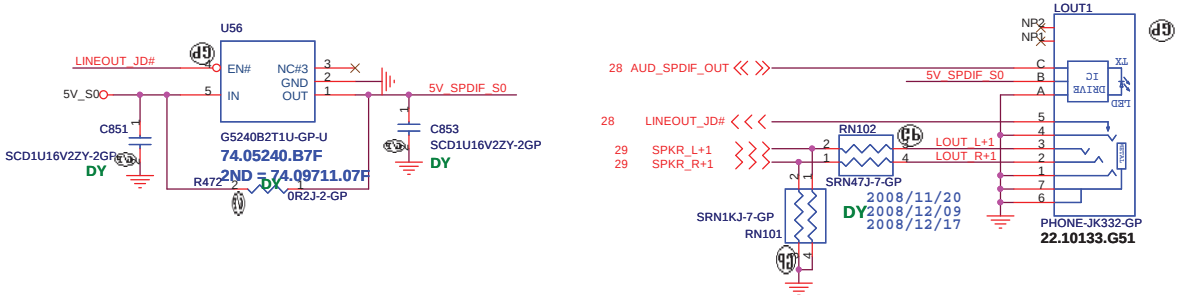
LINE IN



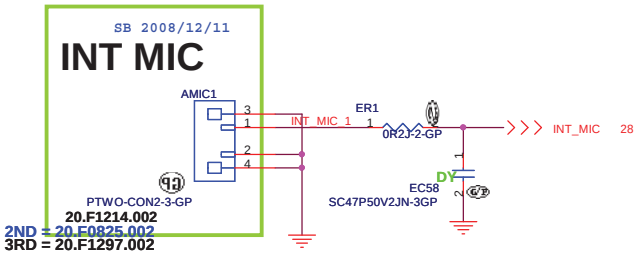
MIC IN



LINE OUT

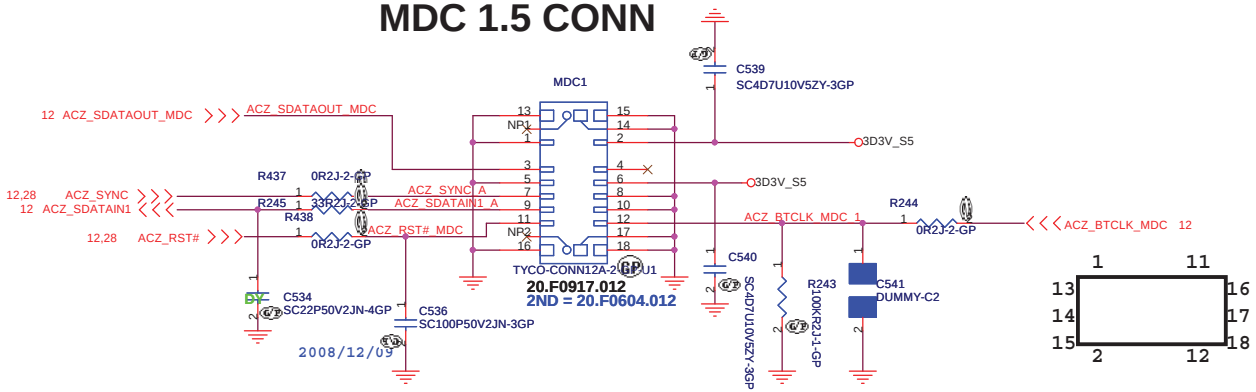


INT MIC



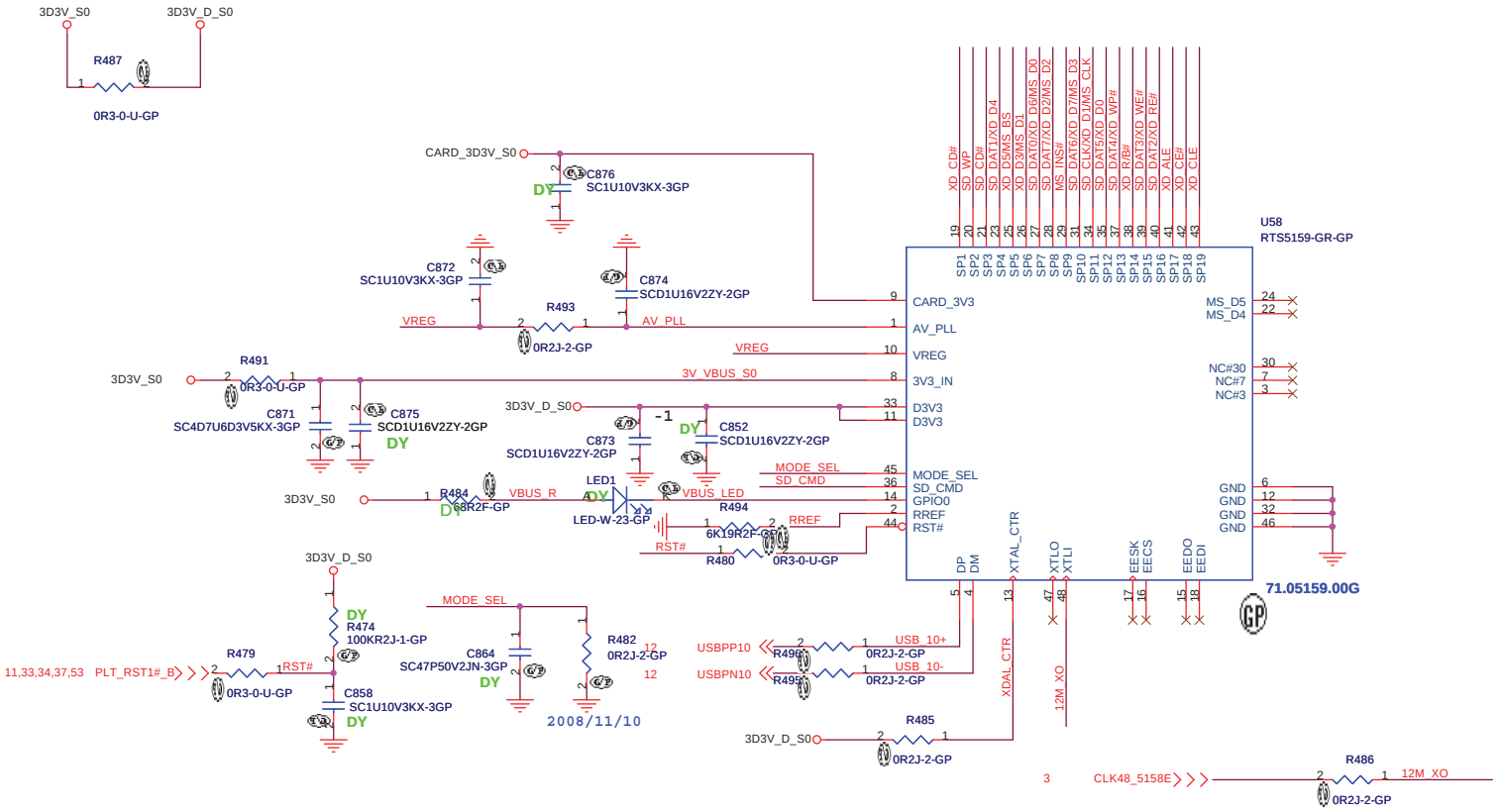
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: AUDIO JACK		
Size	Document Number: JV50-PU	Rev: SB
Date: Friday, December 19, 2008	Sheet 30 of 61	

MDC 1.5 CONN

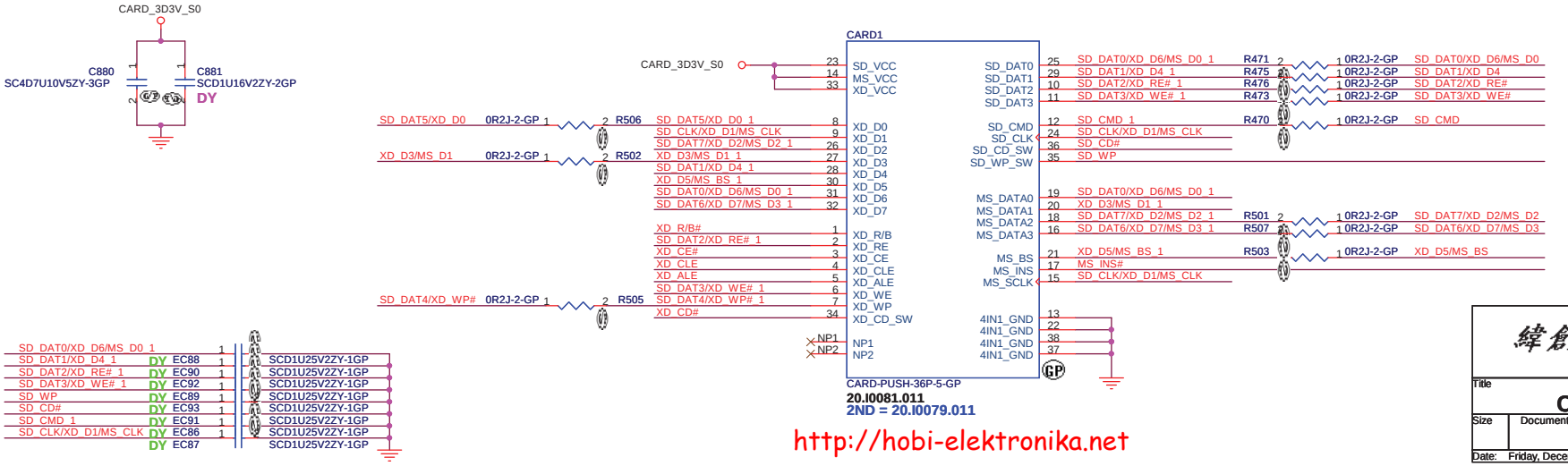


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	MDC	
Size	Document Number JV50-PU	Rev SB
Date: Friday, December 19, 2008	Sheet 31 of 61	

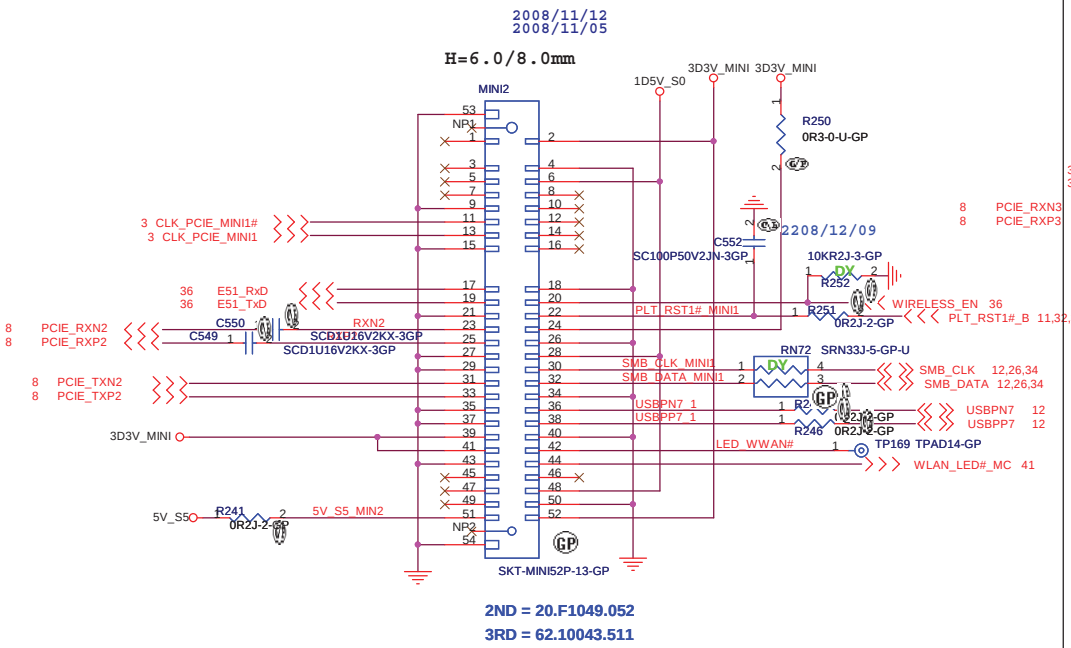


5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CARDREADER- RTS5159**	
Size	Document Number **JV50-PU**	Rev **SB**
Date: Friday, December 19, 2008	Sheet 32 of 61	

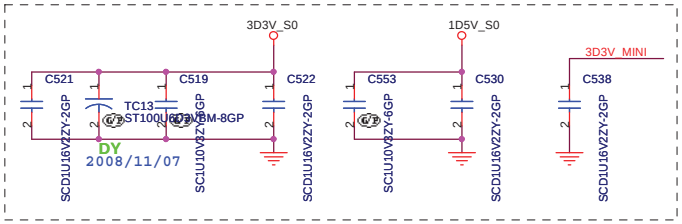
Mini Card Connector(WLAN)



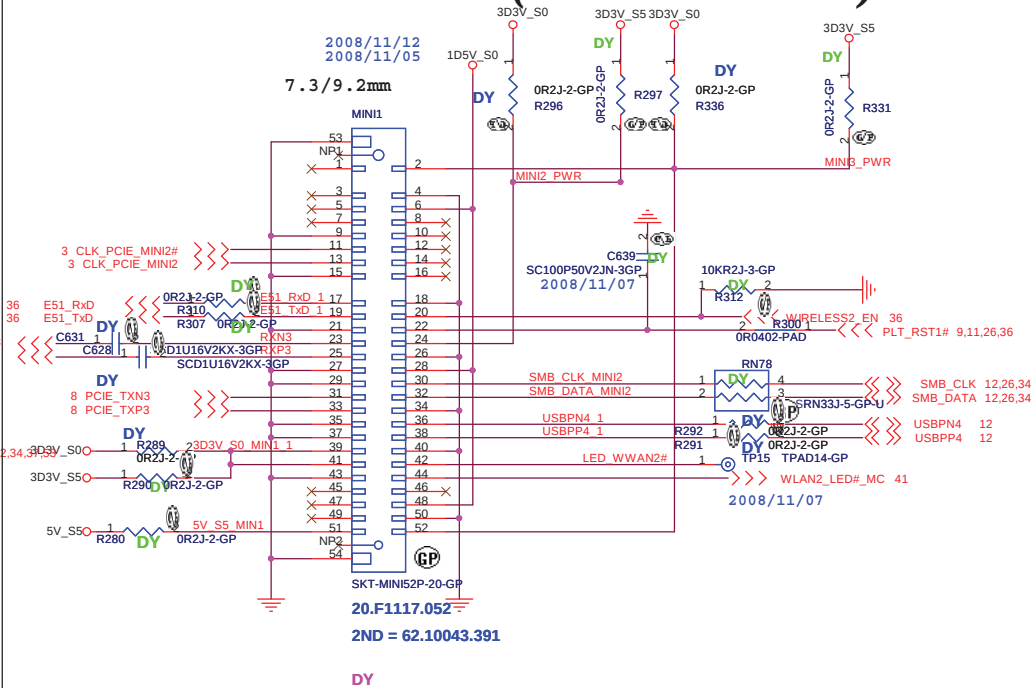
2ND = 20.F1049.052

3RD = 62.10043.511

Place near MINI2



Mini Card Connector(Robson2 and 3G)

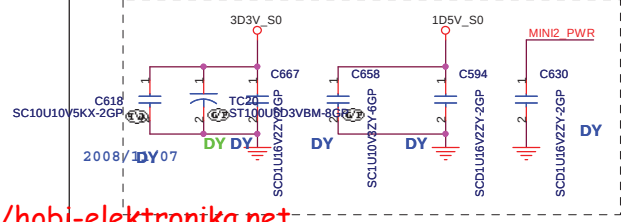


20.F1117.052

2ND = 62.10043.391

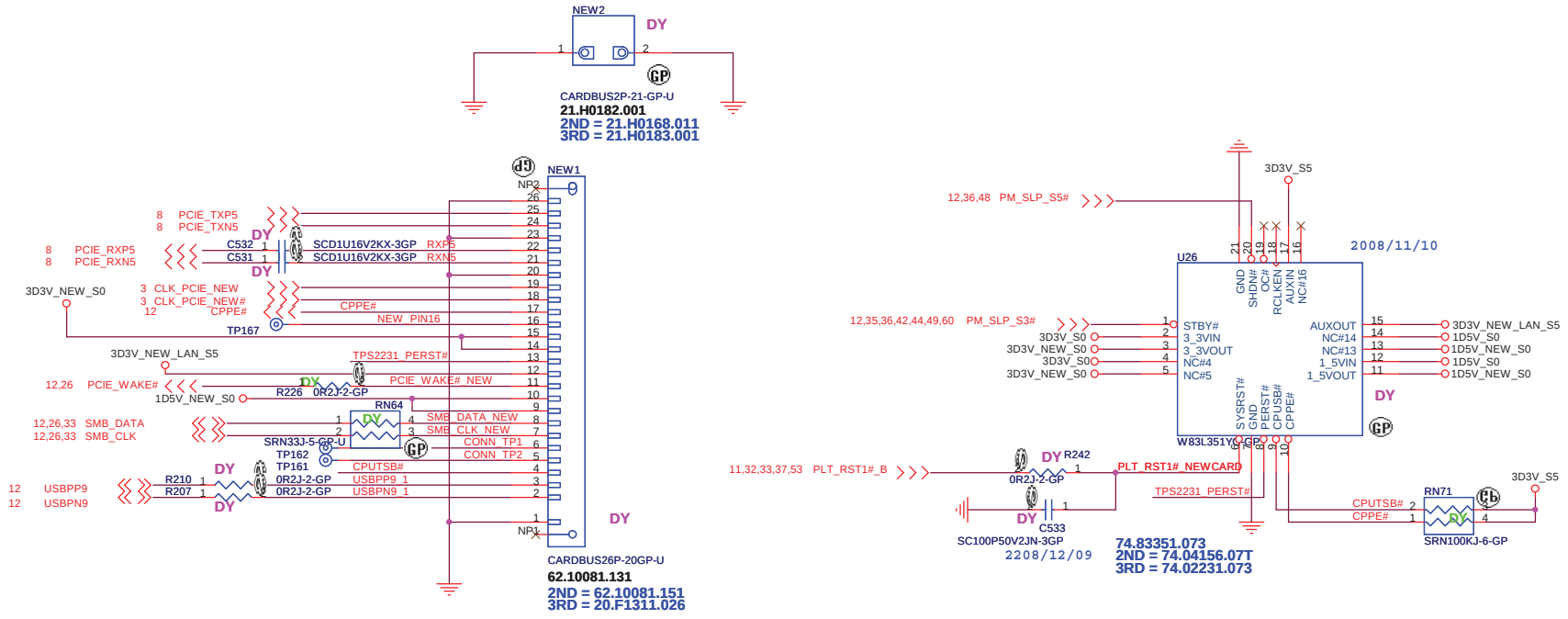
DY

Place near MINI1

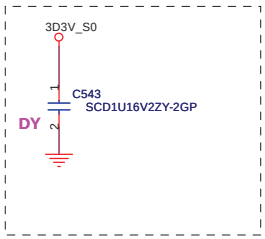


緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**MINI CARD**
Size	Document Number **JV50-PU** Rev **SB**
Date: Friday, December 19, 2008	Sheet 33 of 61

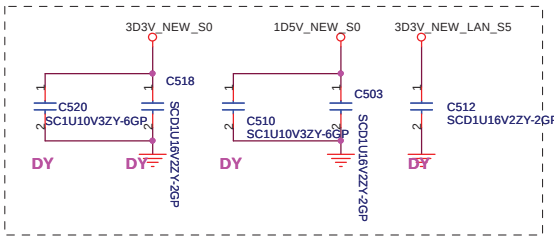
NEWCARD Connector



Place them Near to Chip

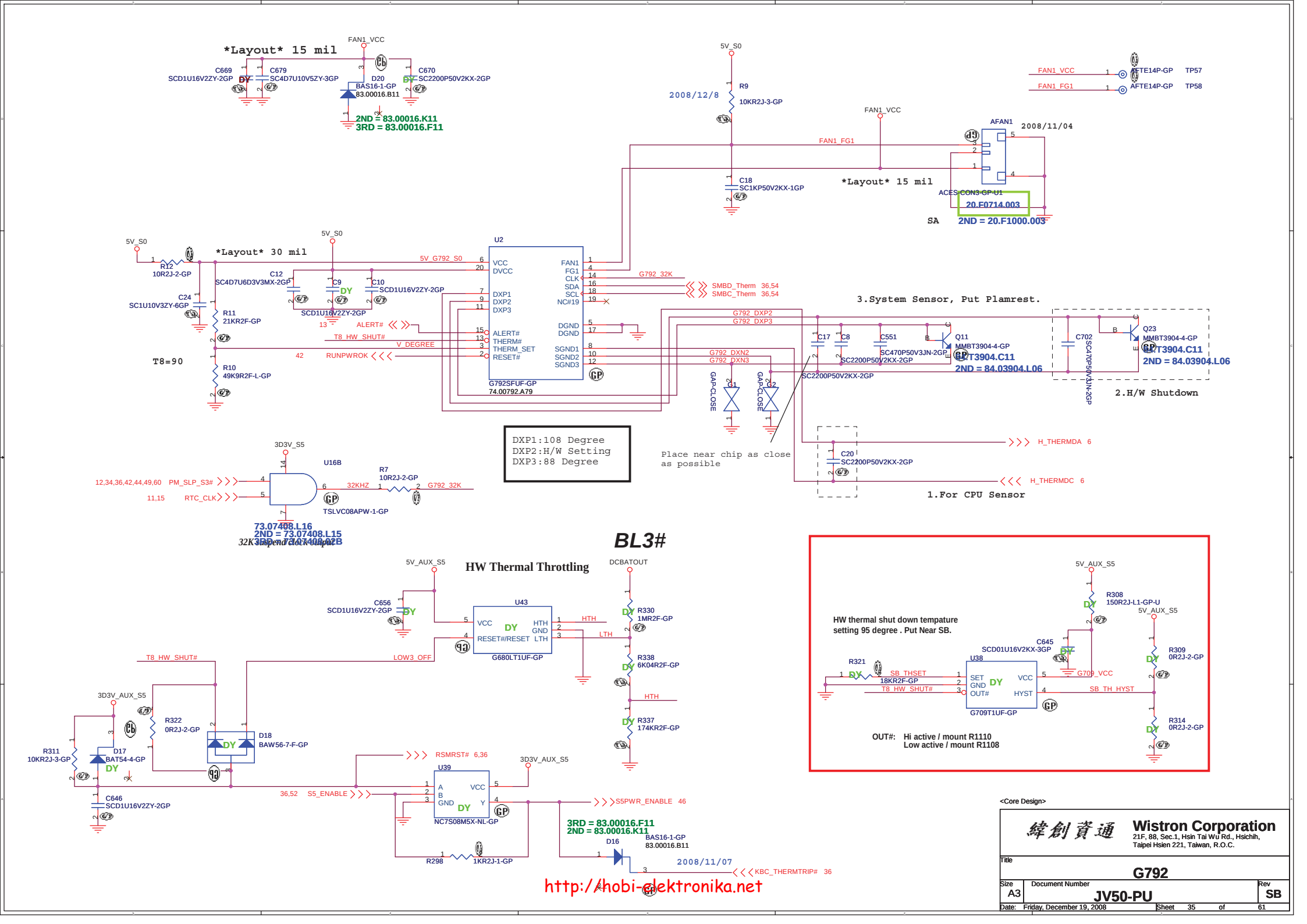


Place them Near to Connector



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

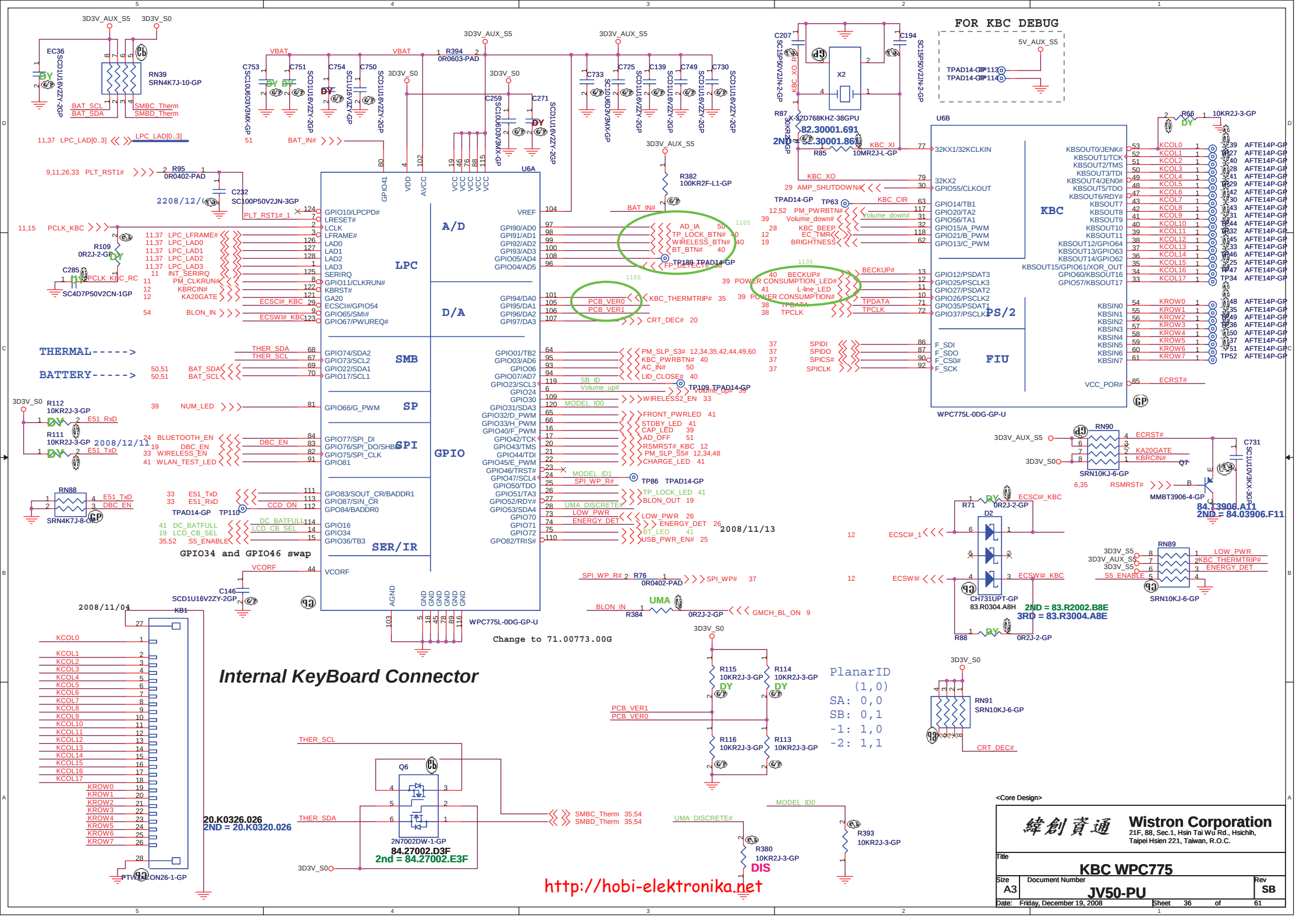
Title: NEW CARD		
Size	Document Number: JV50-PU	Rev: SB
Date: Friday, December 19, 2008	Sheet 34 of 61	

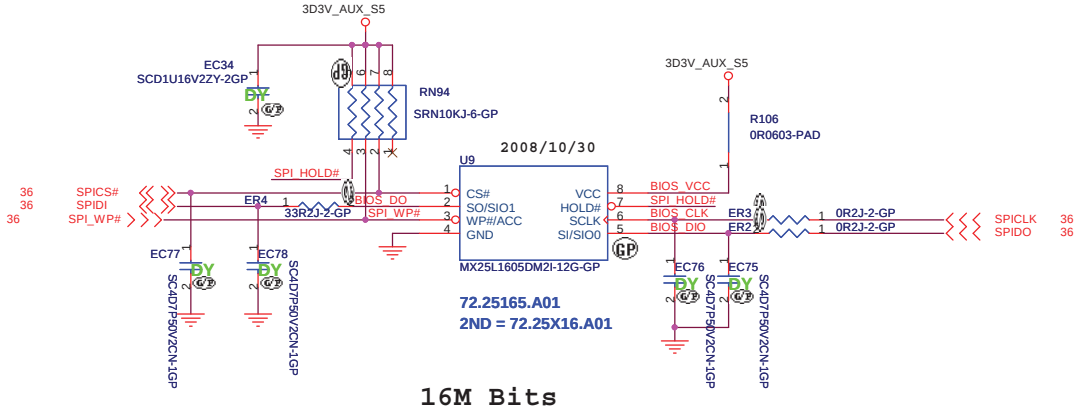


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	G792	
Size A3	Document Number JV50-PU	Rev SB
Date: Friday, December 19, 2008	Sheet 35 of 61	

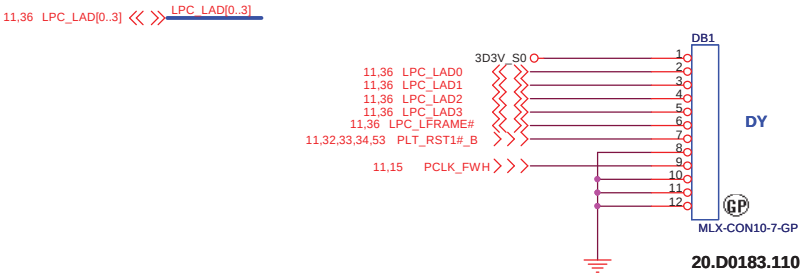

FOR KBC DEBUG
U6A
WPC775L-0DG-GP-U
U6B
WPC775L-0DG-GP-U
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
KBC
PS/2
FIU
THERMAL----->
BATTERY----->
GPIO34 and GPIO46 swap
2008/12/11
2008/11/04
2008/11/13
Change to 71.00773.00G
Internal KeyBoard Connector
UMA
DIS
PlanarID
(1,0)
SA: 0,0
SB: 0,1
-1: 1,0
-2: 1,1
20.K0326.026
2ND = 20.K0320.026
84.27002.D3F
2nd = 84.27002.E3F
82.30001.691
2ND = 82.30001.861
84.03906.A11
2ND = 84.03906.F11
2ND = 83.R2002.B8E
3RD = 83.R3004.A8E
http://hobi-elektronika.net
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC775
JV50-PU
Size A3
Rev SB
Date: Friday, December 19, 2008
Sheet 36 of 61



16M Bits

SPI FLASH ROM

GOLDEN FINGER FOR DEBUG BOARD



<Core Design>

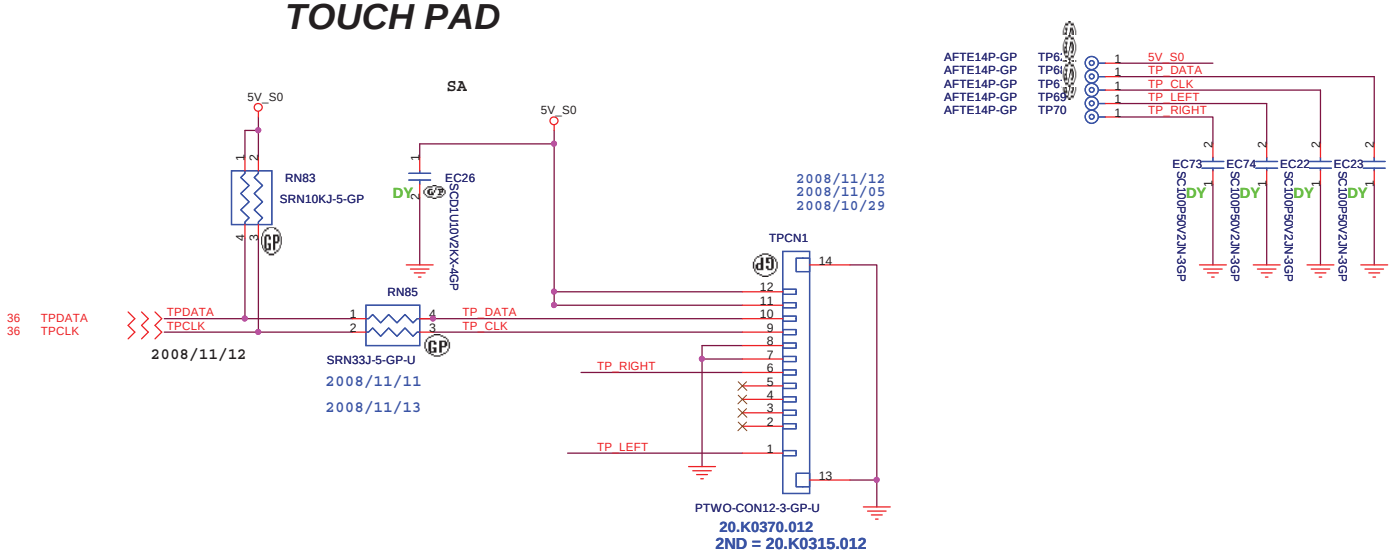
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS

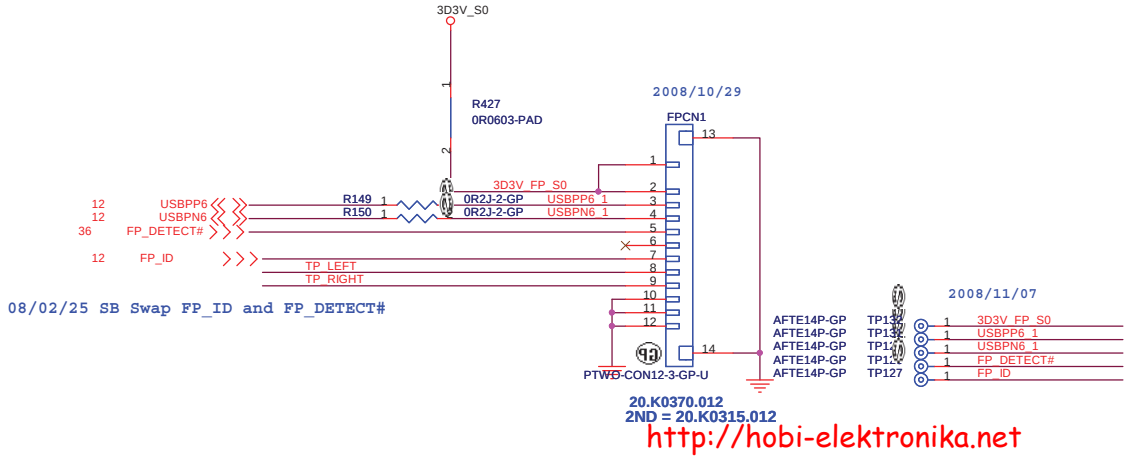
Size: A3 | Document Number: JV50-PU | Rev: SB

Date: Friday, December 19, 2008 | Sheet 37 of 61

TOUCH PAD



Finger printer



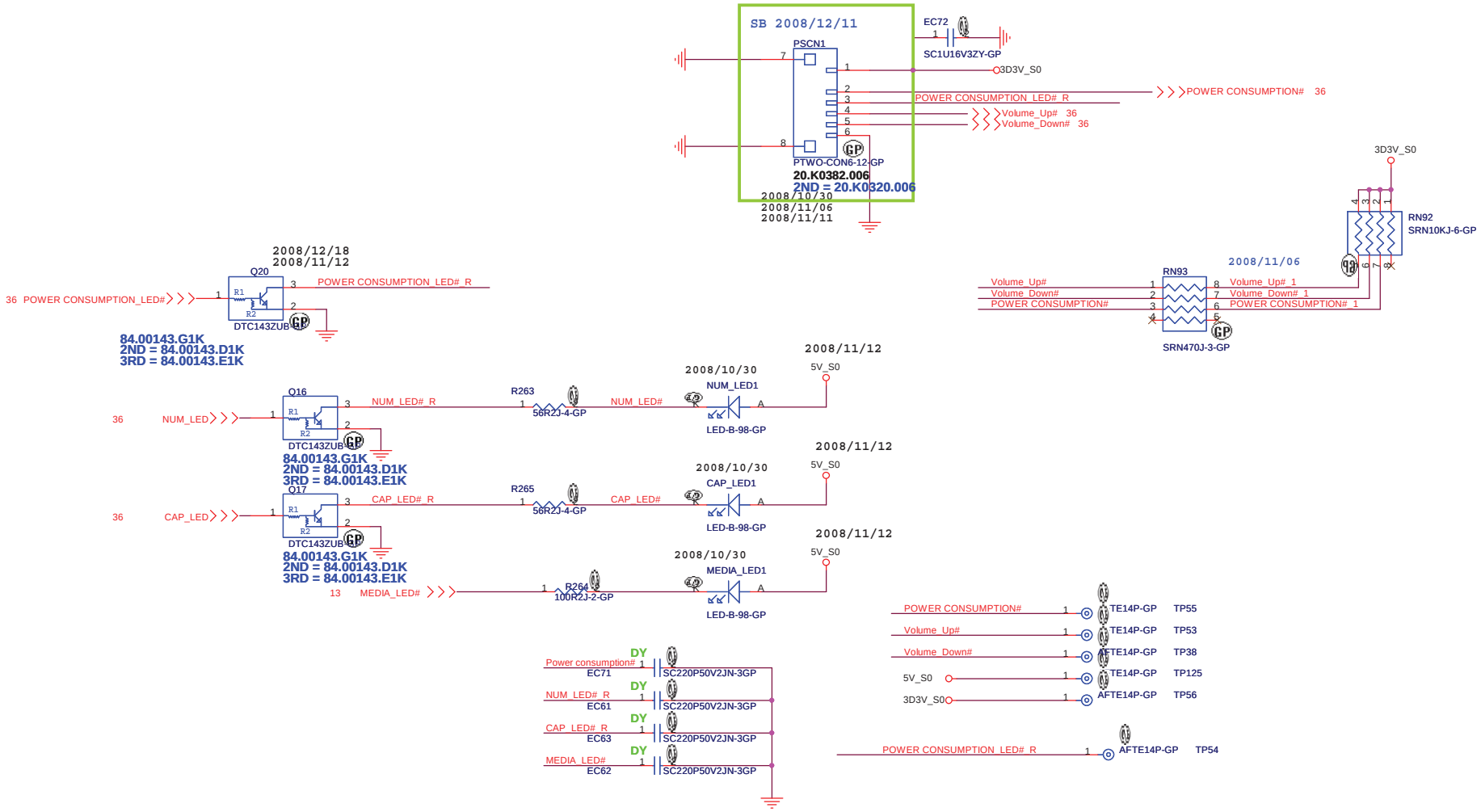
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Touch PAD/Finger printer

Size	Document Number	Rev
A3	JV50-PU	SB

Date: Friday, December 19, 2008 Sheet 38 of 61

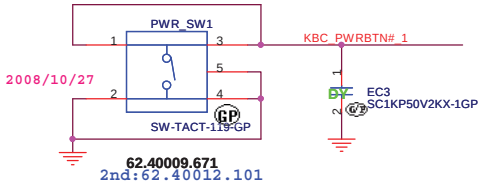


http://hobi-elektronika.net

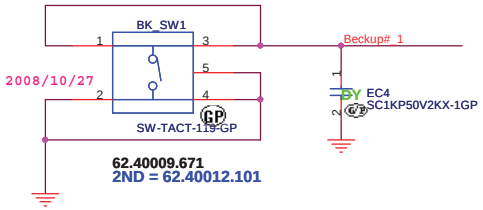
緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: LAUNCH BOARD		
Size: A3	Document Number: JV50-PU	Rev: SB
Date: Friday, December 19, 2008	Sheet 39 of 61	

Cover Up Switch

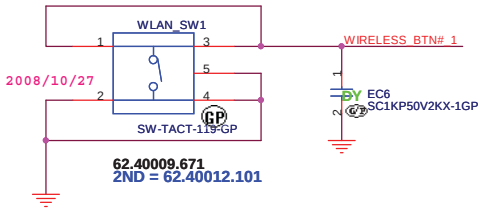
Power Button



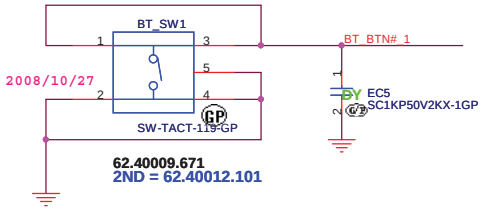
Beckup Button

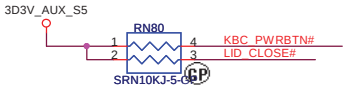


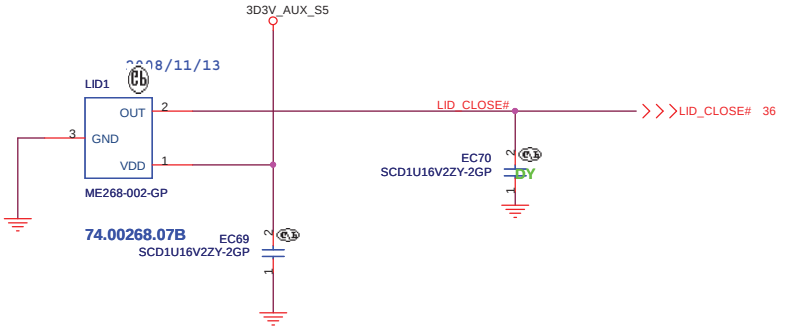
WIRELESS Button

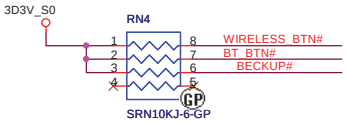


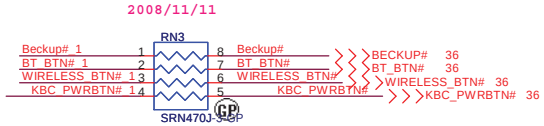
BT/3G Button



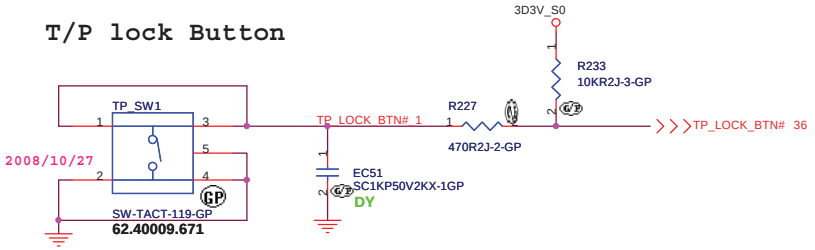






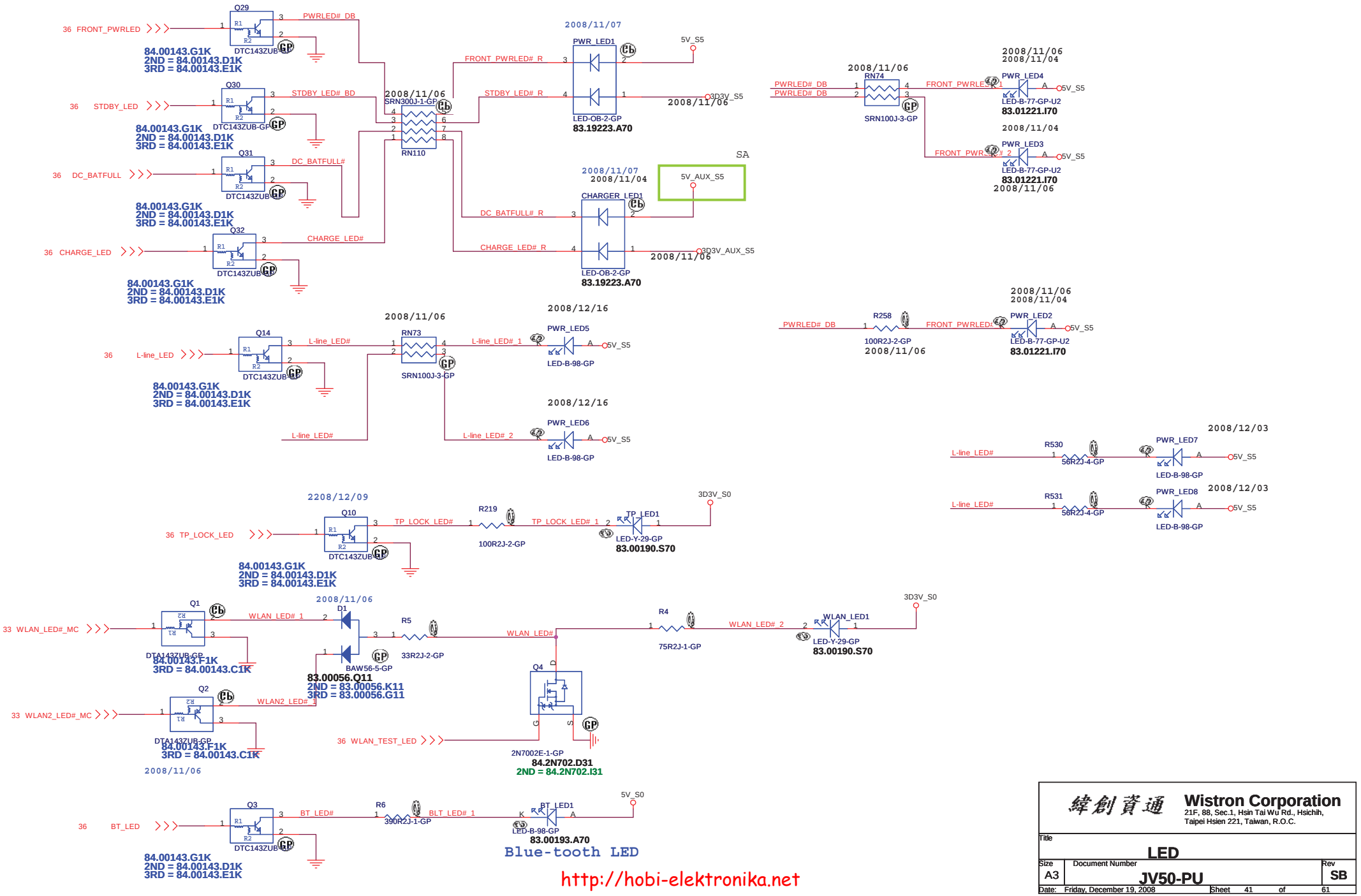


T/P lock Button

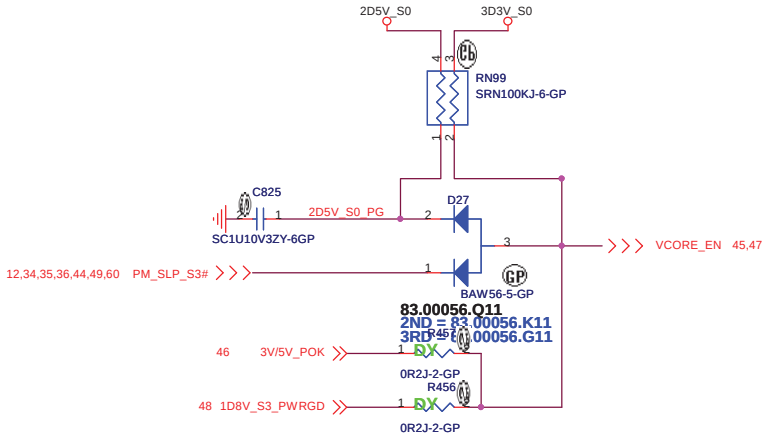


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

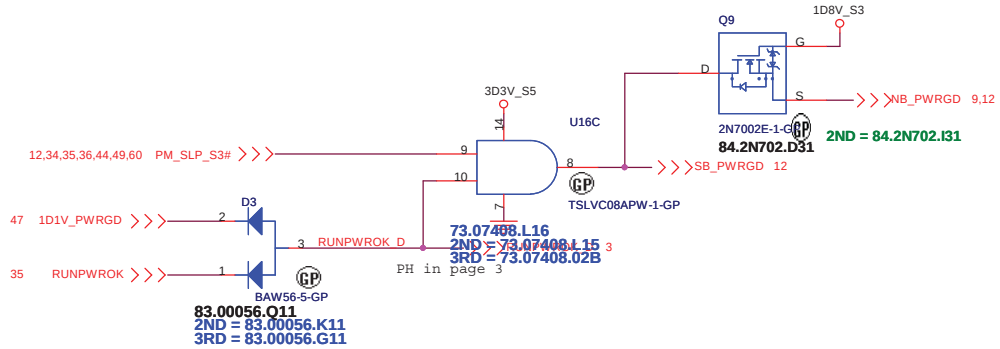
Title	SWITCH	
Size: A3	Document Number: JV50-PU	Rev: SB
Date: Friday, December 19, 2008	Sheet 40 of 61	



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LED	
Size: A3	Document Number: JV50-PU	Rev: SB
Date: Friday, December 19, 2008	Sheet 41 of 61	



P/H @ 1D8V_S3 PAGE



<Core Design>

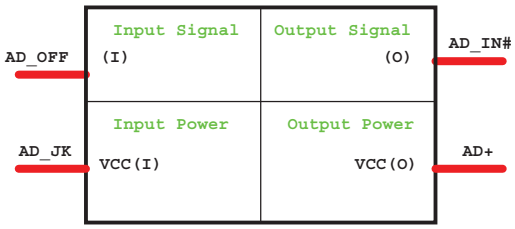
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER ON LOGIC

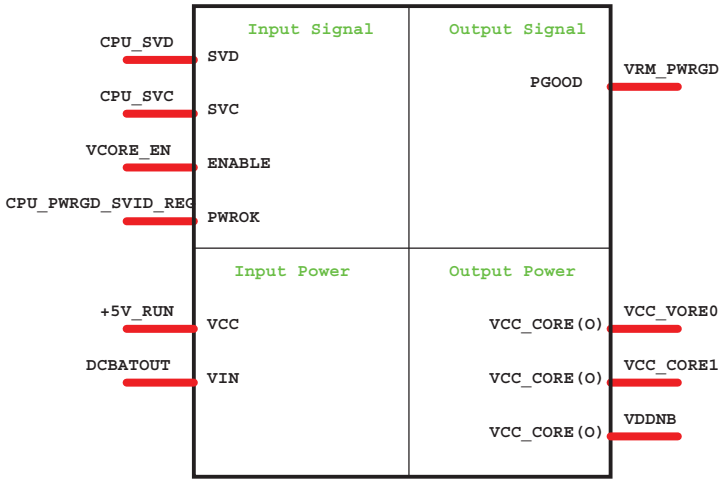
Size: A3 | Document Number: JV50-PU | Rev: SB

Date: Friday, December 19, 2008 | Sheet 42 of 61

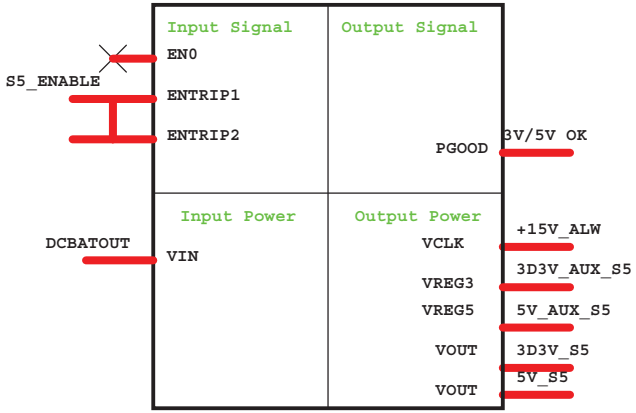
Adapter



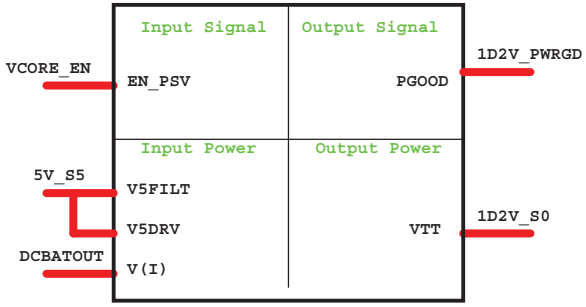
CPU_CORE
ISL6265HRTZ



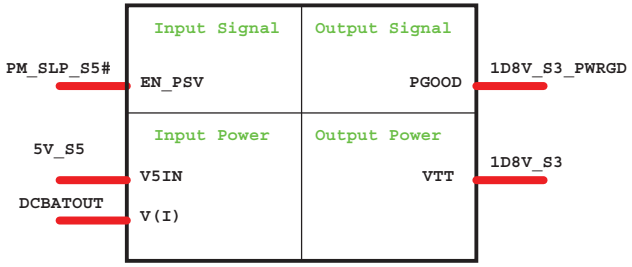
DCDC 5V/3D3V(TPS51125)



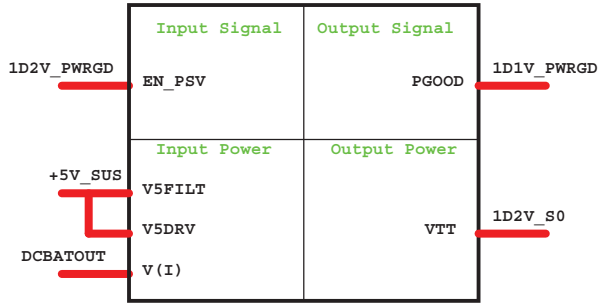
DCDC 1D2V(RT8202)



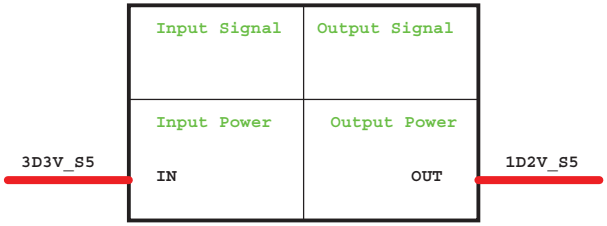
DCDC 1D8V(RT8202)



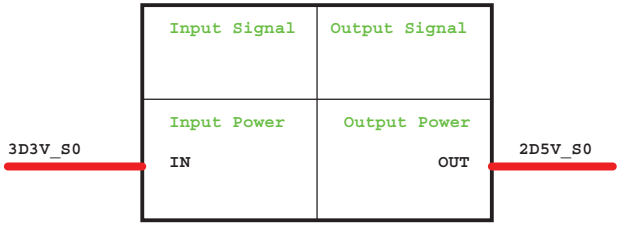
DCDC 1D1V(RT8202)



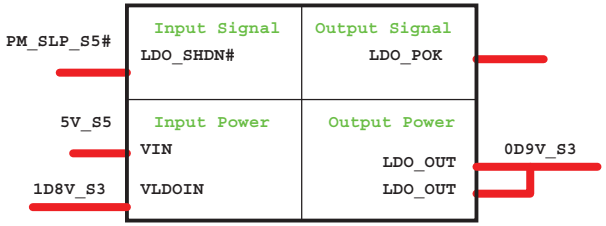
1D2V LDO G9161



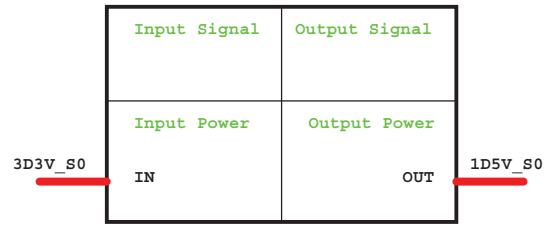
2D5V LDO R9161



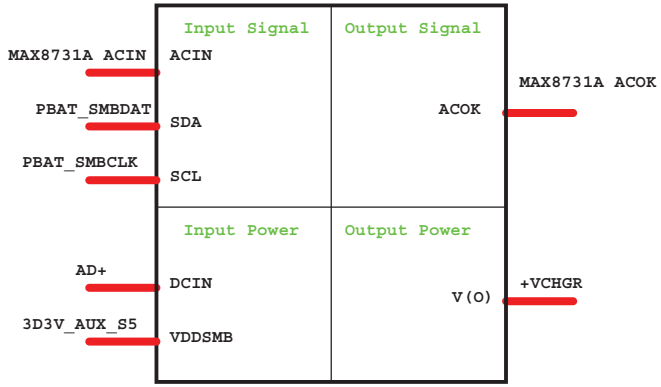
0D9V LDO RT9026



1D5V LDO G9571



CHARGER MAX8731



<Core Design>

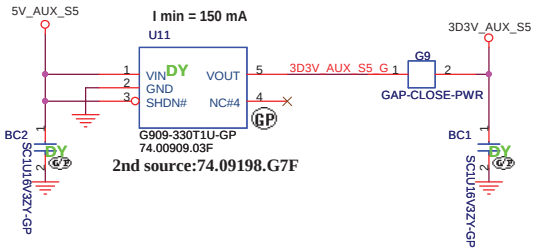
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

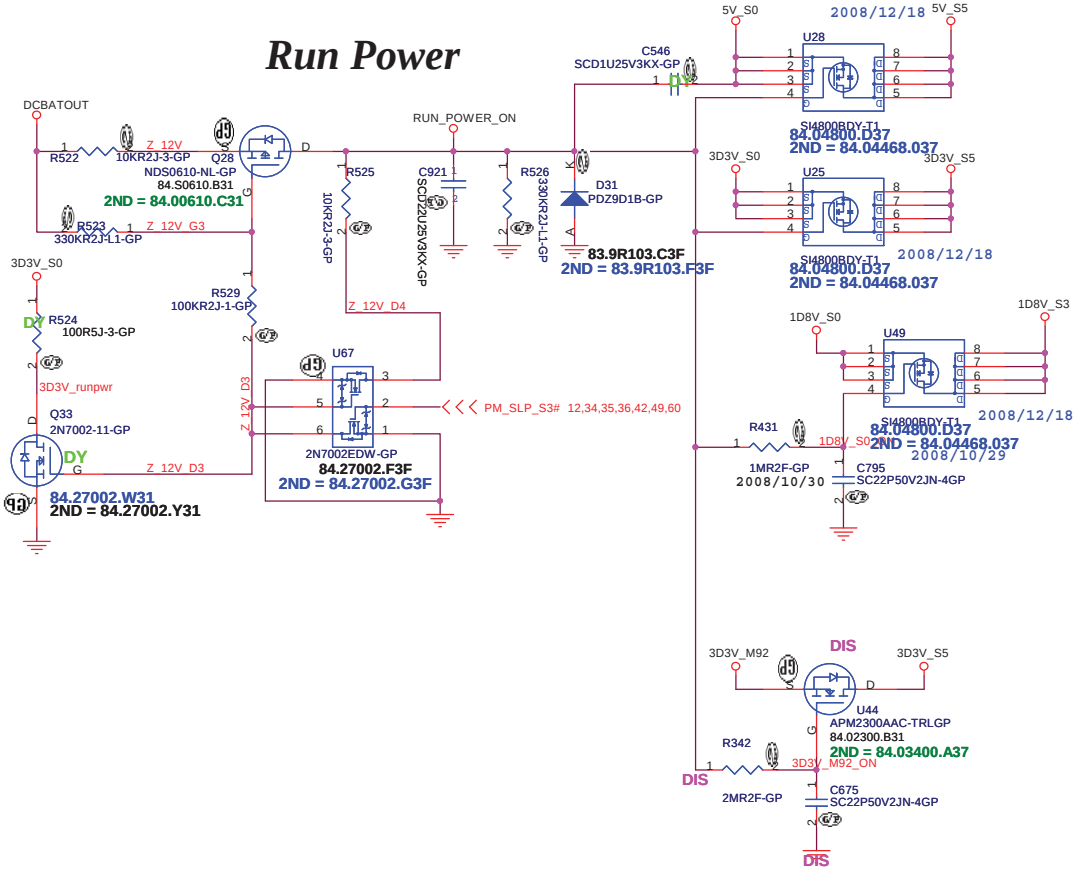
Size	Document Number	Rev
A3	JV50-PU	SB

Date: Friday, December 19, 2008 Sheet 43 of 61

Aux Power 3D3V_AUX_S5



Run Power



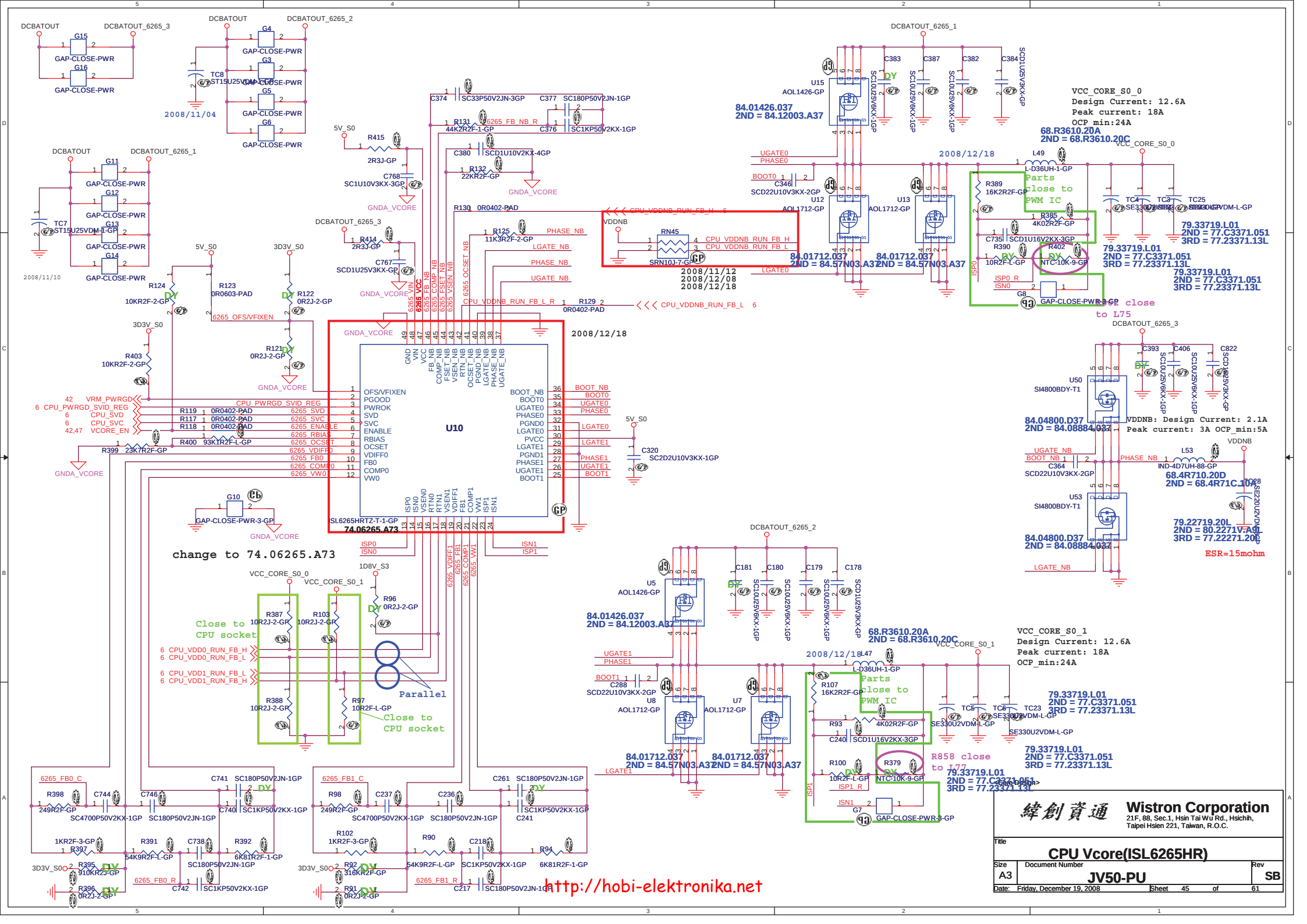
<Core Design>

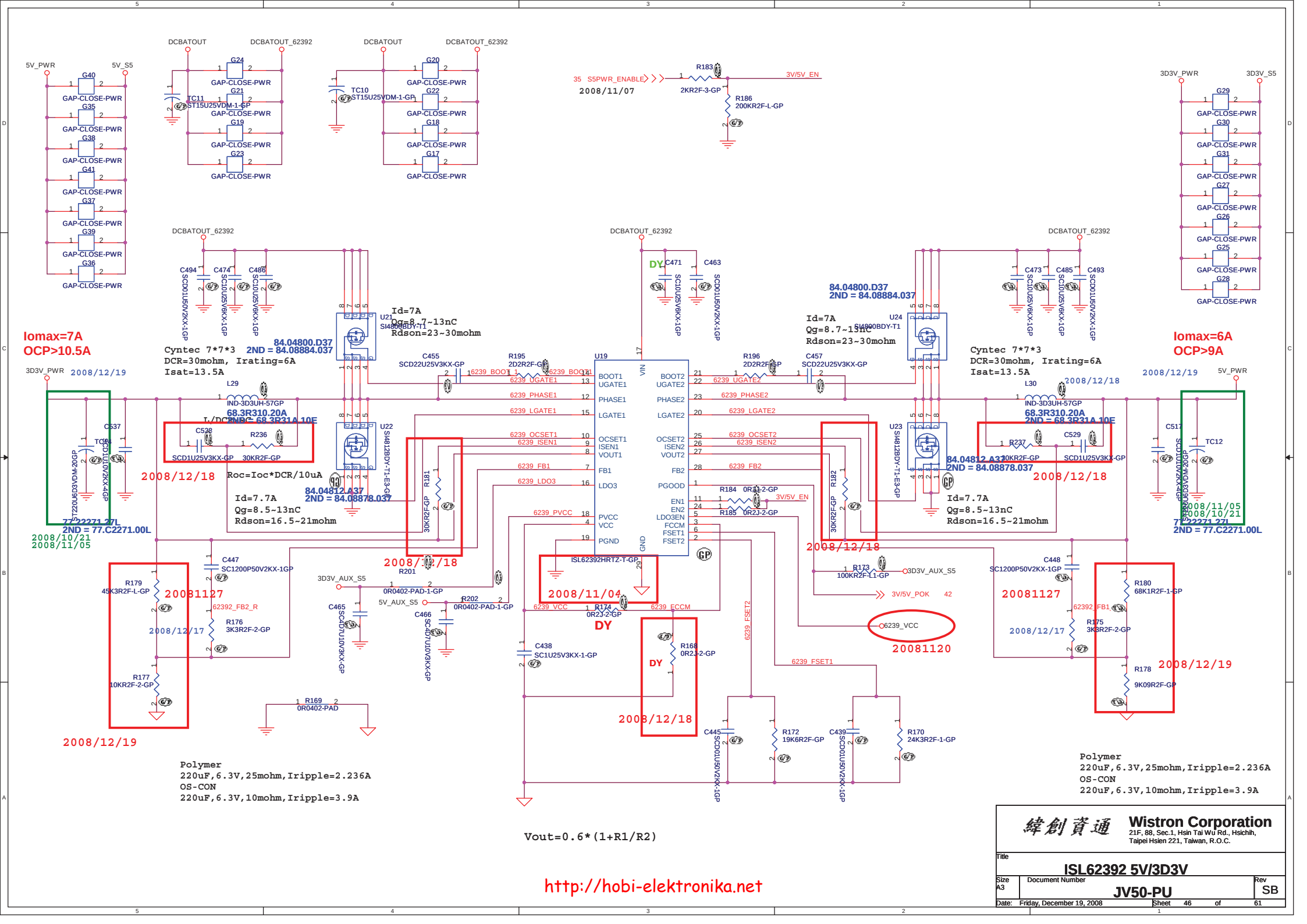
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

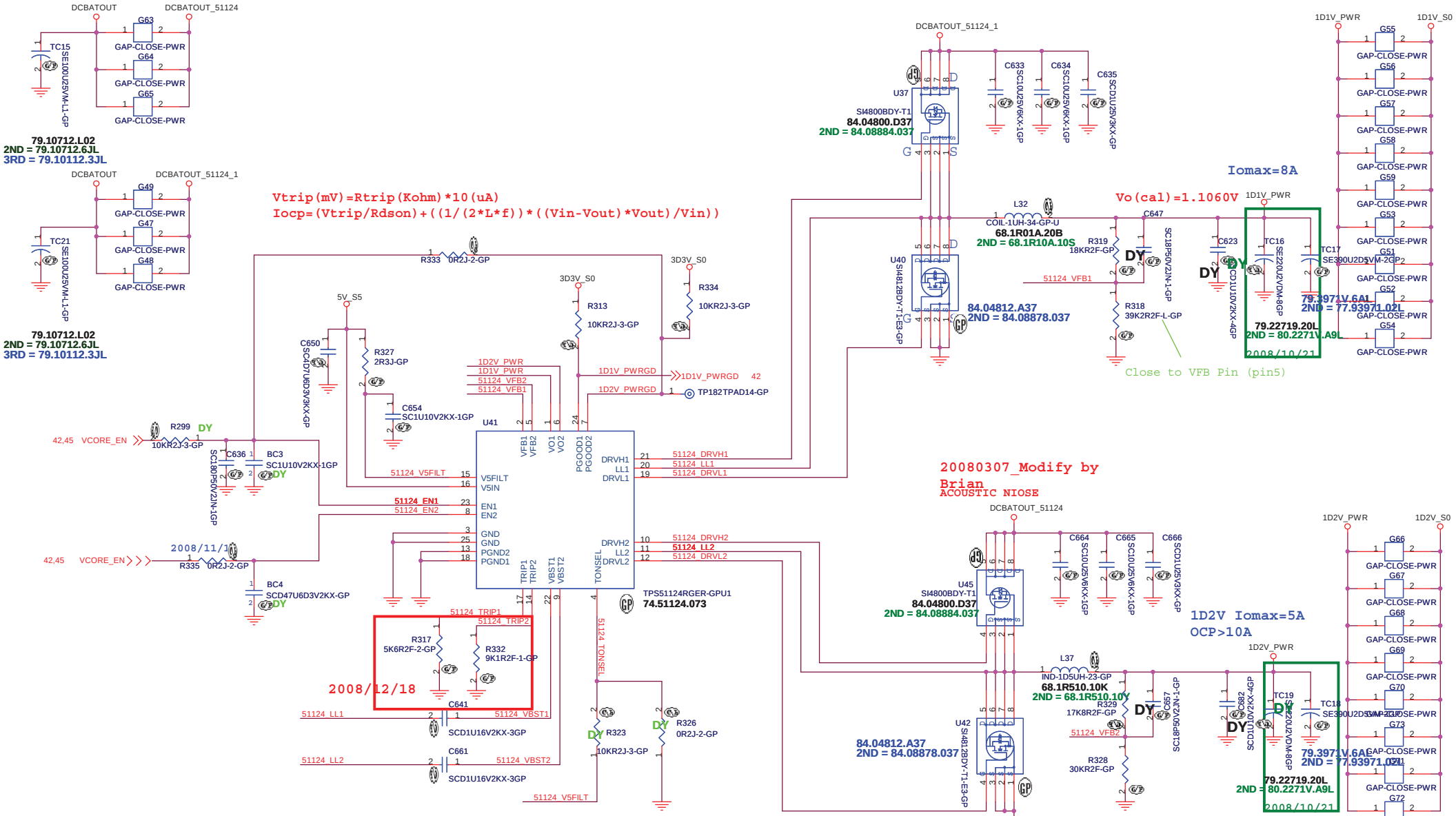
Title: RUN AND AUX POWER

Size	Document Number	Rev
A3	JV50-PU	SB

Date: Friday, December 19, 2008 Sheet 44 of 61


U10
SL6265HRTZ-T-1-GP
74.06265.A73
change to 74.06265.A73
U15
AOL1426-GP
U12
AOL1712-GP
U13
AOL1712-GP
U5
AOL1426-GP
U8
AOL1712-GP
U7
AOL1712-GP
U50
SI4800BDY-T1
U53
SI4800BDY-T1
VCC_CORE_S0_0
Design Current: 12.6A
Peak current: 18A
OCP min:24A
VCC_CORE_S0_1
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VDDNB: Design Current: 2.1A
Peak current: 3A OCP_min:5A
84.01426.037
2ND = 84.12003.A37
84.01712.037
2ND = 84.57N03.A37
84.04800.D37
2ND = 84.08884.037
68.R3610.20A
2ND = 68.R3610.20C
68.4R710.20D
2ND = 68.4R71C.10A
79.33719.L01
2ND = 77.C3371.051
3RD = 77.23371.13L
79.22719.20L
2ND = 80.22717.A3L
3RD = 77.22271.20L
ESR=15mohm
Close to CPU socket
Parallel
Parts close to PWM IC
R858 close to L77
R3 close to L75
2008/11/04
2008/11/10
2008/11/12
2008/12/08
2008/12/18
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore(ISL6265HR)
JV50-PU
Size A3
Rev SB
Date: Friday, December 19, 2008
Sheet 45 of 61
http://hobi-elektronika.net


5V_PWR
5V_S5
3D3V_PWR
3D3V_S5
DCBATOUT
DCBATOUT_62392
GAP-CLOSE-PWR
35 S5PWR_ENABLE
2008/11/07
R183
2KR2F-3-GP
3V/5V_EN
R186
200KR2F-L-GP
Iomax=7A
OCP>10.5A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
84.04800.D37
2ND = 84.08884.037
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
U21
SI4800BDY-T1
U24
U19
ISL62392HRTZ-T-GP
Iomax=6A
OCP>9A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
L29
IND-3D3UH-57GP
68.3R310.20A
2ND = 68.3R31A.10E
L30
U22
SI4812BDY-T1-E3-GP
U23
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
84.04812.A37
2ND = 84.08878.037
Roc=Ioc*DCR/10uA
2008/12/18
2008/12/19
2008/11/05
2008/10/21
77.C2271.27L
2ND = 77.C2271.00L
2008/11/04
2008/12/17
20081127
20081120
DY
3V/5V_POK
3D3V_AUX_S5
5V_AUX_S5
6239_VCC
6239_FCCM
6239_FSET1
6239_FB1
Vout=0.6*(1+R1/R2)
Polymer
220uF,6.3V,25mohm,Iripple=2.236A
OS-CON
220uF,6.3V,10mohm,Iripple=3.9A
http://hobi-elektronika.net
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL62392 5V/3D3V
Size A3
Document Number
JV50-PU
Rev SB
Date: Friday, December 19, 2008
Sheet 46 of 61



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

http://hobi-elektronika.net

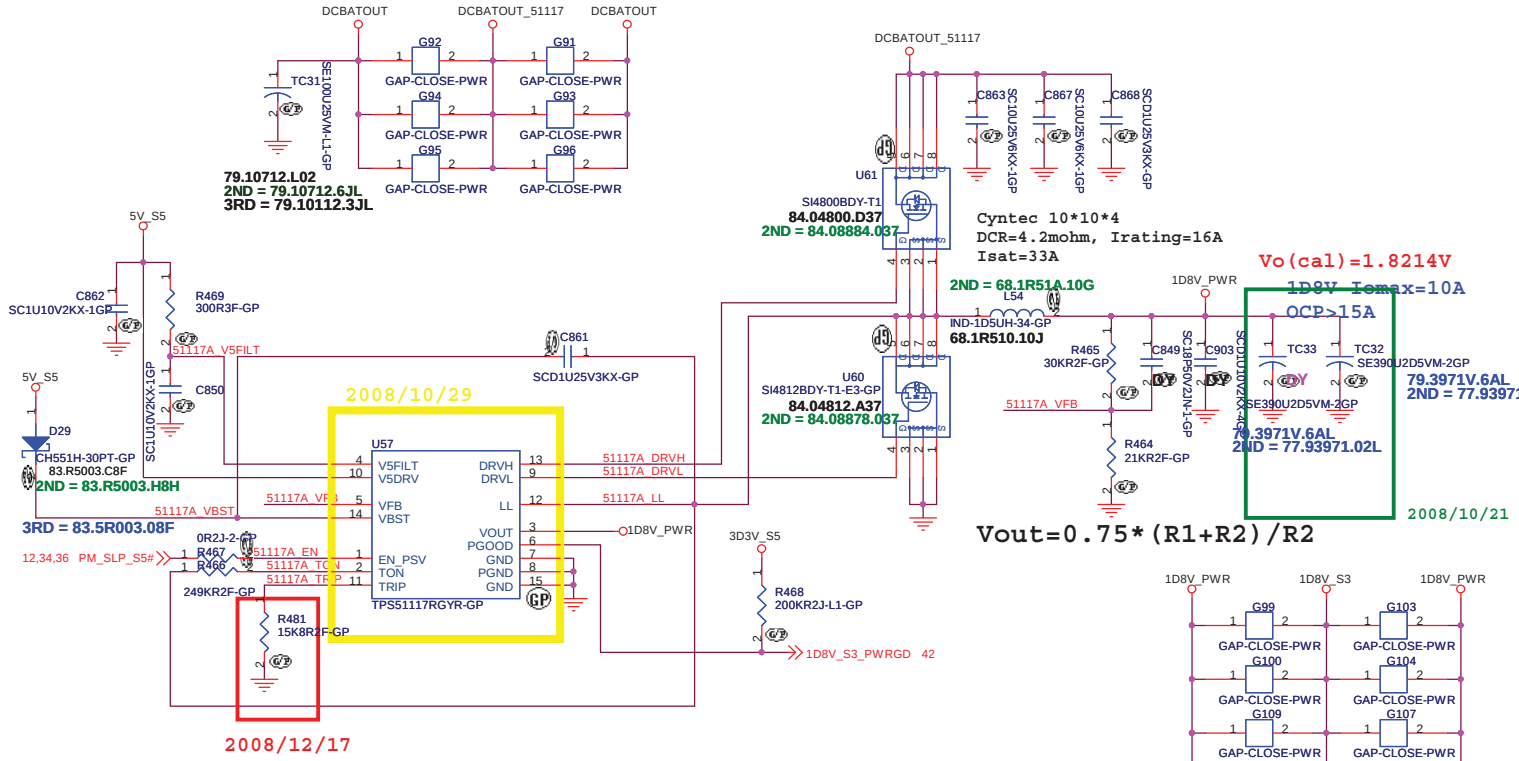
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

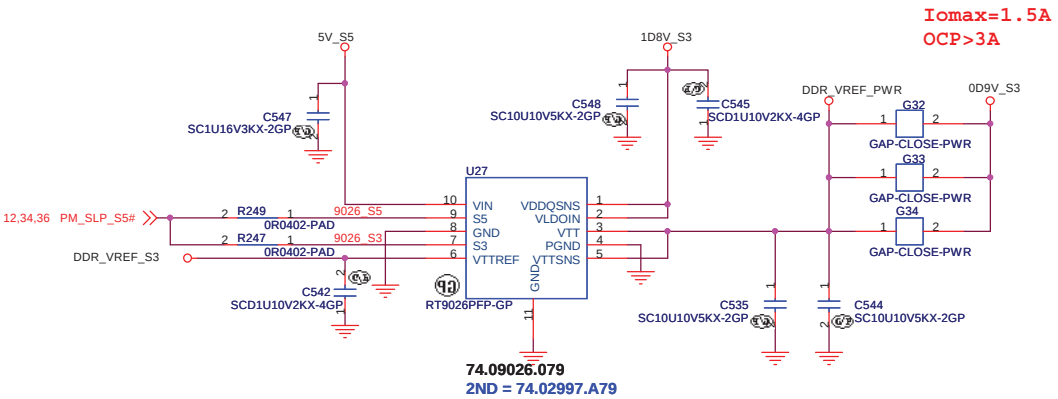
Title: TPS51124_1D1V_1D2V

Size	Document Number	Rev
A3	JV50-PU	SB

Date: Friday, December 19, 2008 Sheet 47 of 61



DDR_0.9V



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

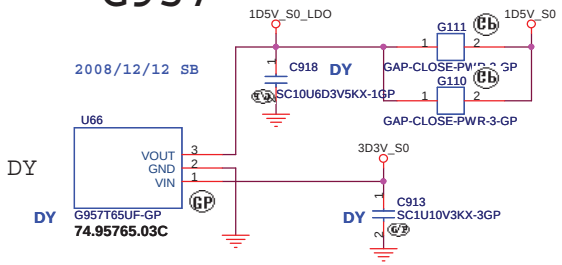
Title: DCDC_1D8V_TPS51117/LDO 0D9V

Size	Document Number	Rev
A3	JV50-PU	SB

Date: Friday, December 19, 2008 Sheet 48 of 61

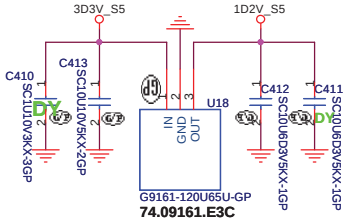
1D5V_S0
Iomax=1A

G957



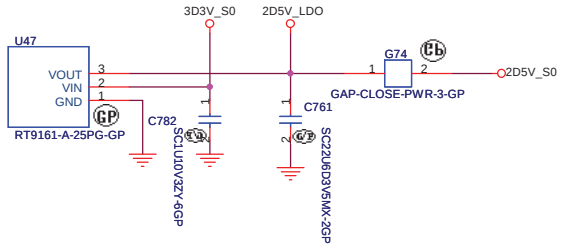
For MINI Card.NEW Card power SW

1D2V_S5
Iomax=400mA



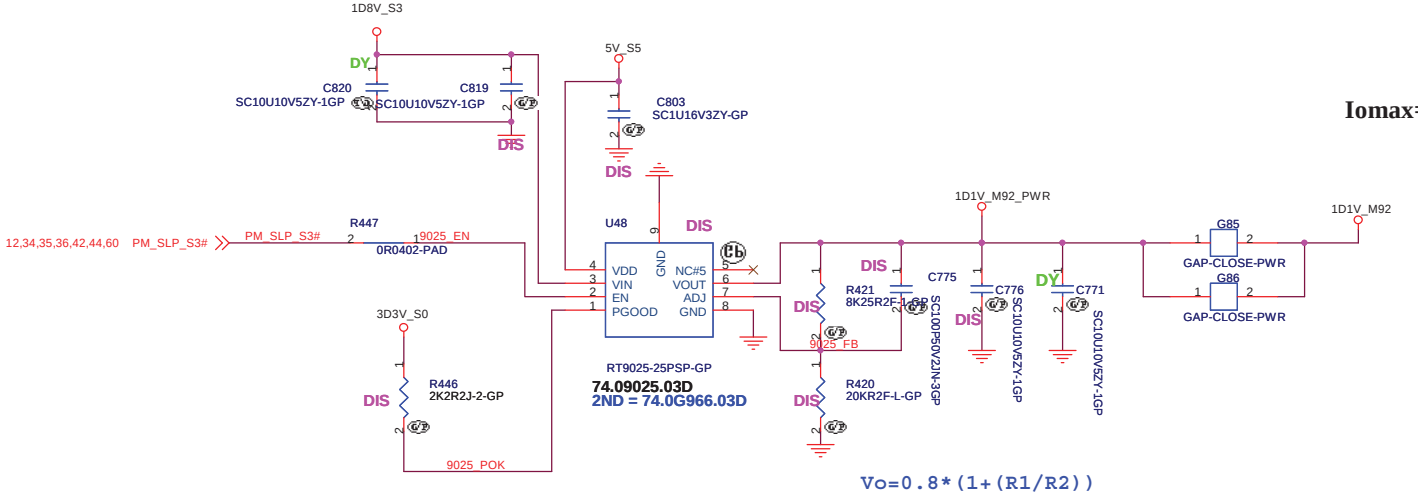
Place near to SB700

2D5V
Iomax=0.2A



Place near to CPU

Iomax=0.8A



Vo=0.8*(1+(R1/R2))

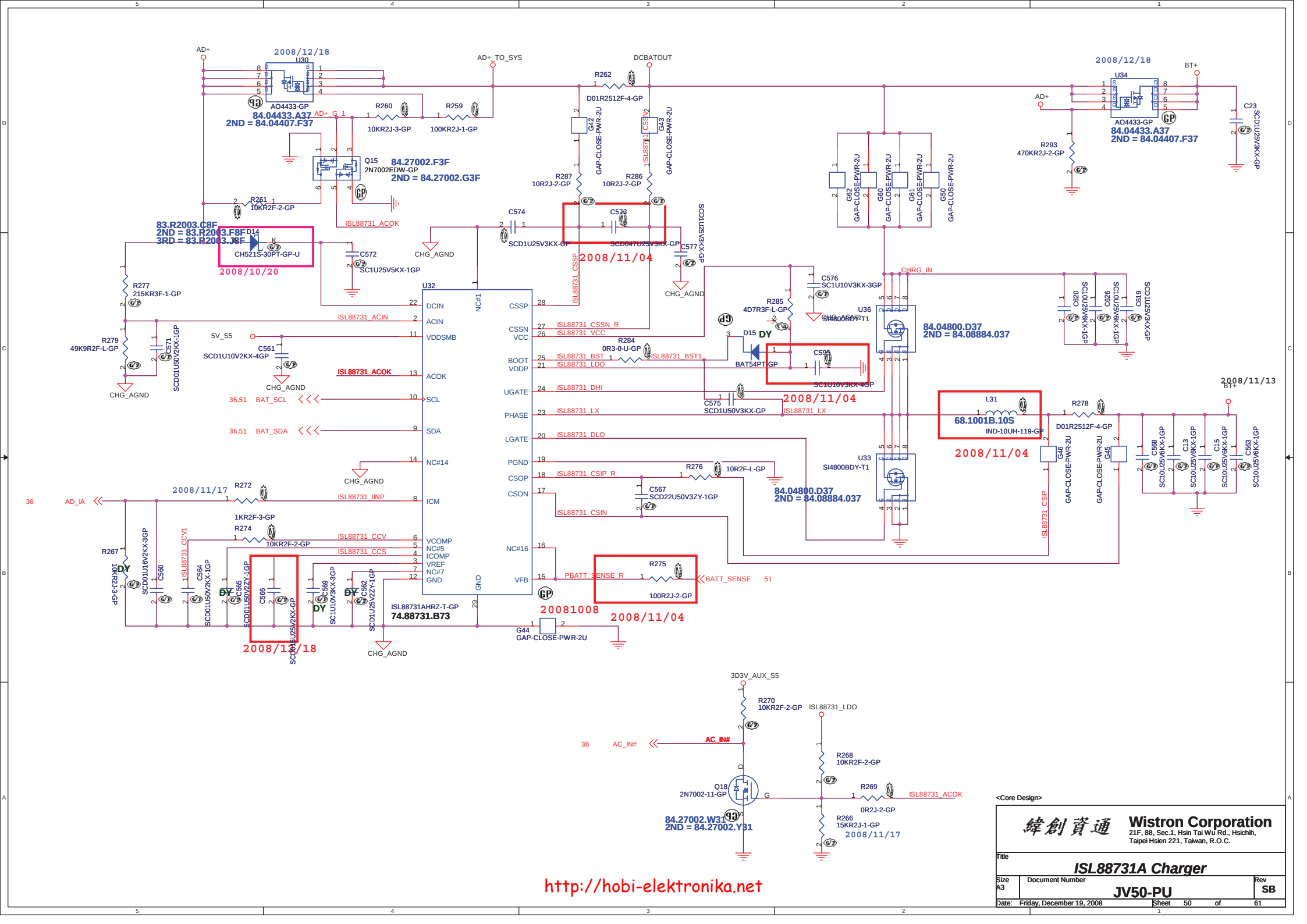
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LDO 2D5V/1D5V/1D2V_S5

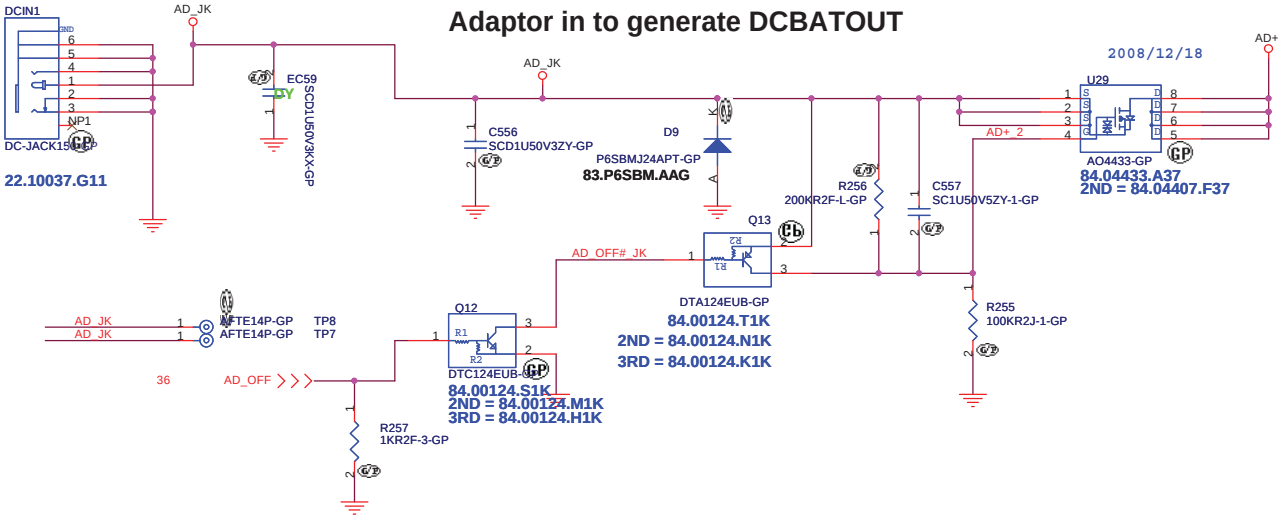
Size	Document Number	Rev
A3	JV50-PU	SB

Date: Friday, December 19, 2008 Sheet 49 of 61

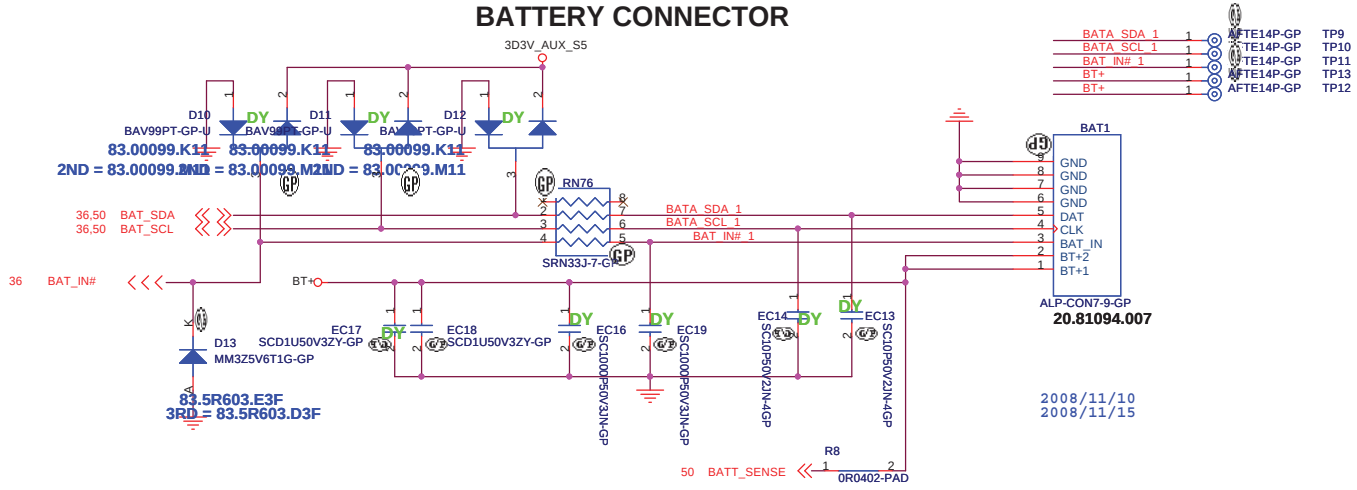

ISL88731AHRZ-T-GP
74.88731.B73
84.04433.A37
2ND = 84.04407.F37
84.27002.F3F
2ND = 84.27002.G3F
83.R2003.C8F
2ND = 83.R2003.F8F
3RD = 83.R2003.J8F
84.04800.D37
2ND = 84.08884.037
84.27002.W31
2ND = 84.27002.Y31
2008/12/18
2008/11/04
2008/11/17
2008/10/20
2008/11/13
20081008
http://hobi-elektronika.net
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL88731A Charger
JV50-PU
Friday, December 19, 2008

2008/11/06
2008/10/29

Adaptor in to generate DCBATOUT

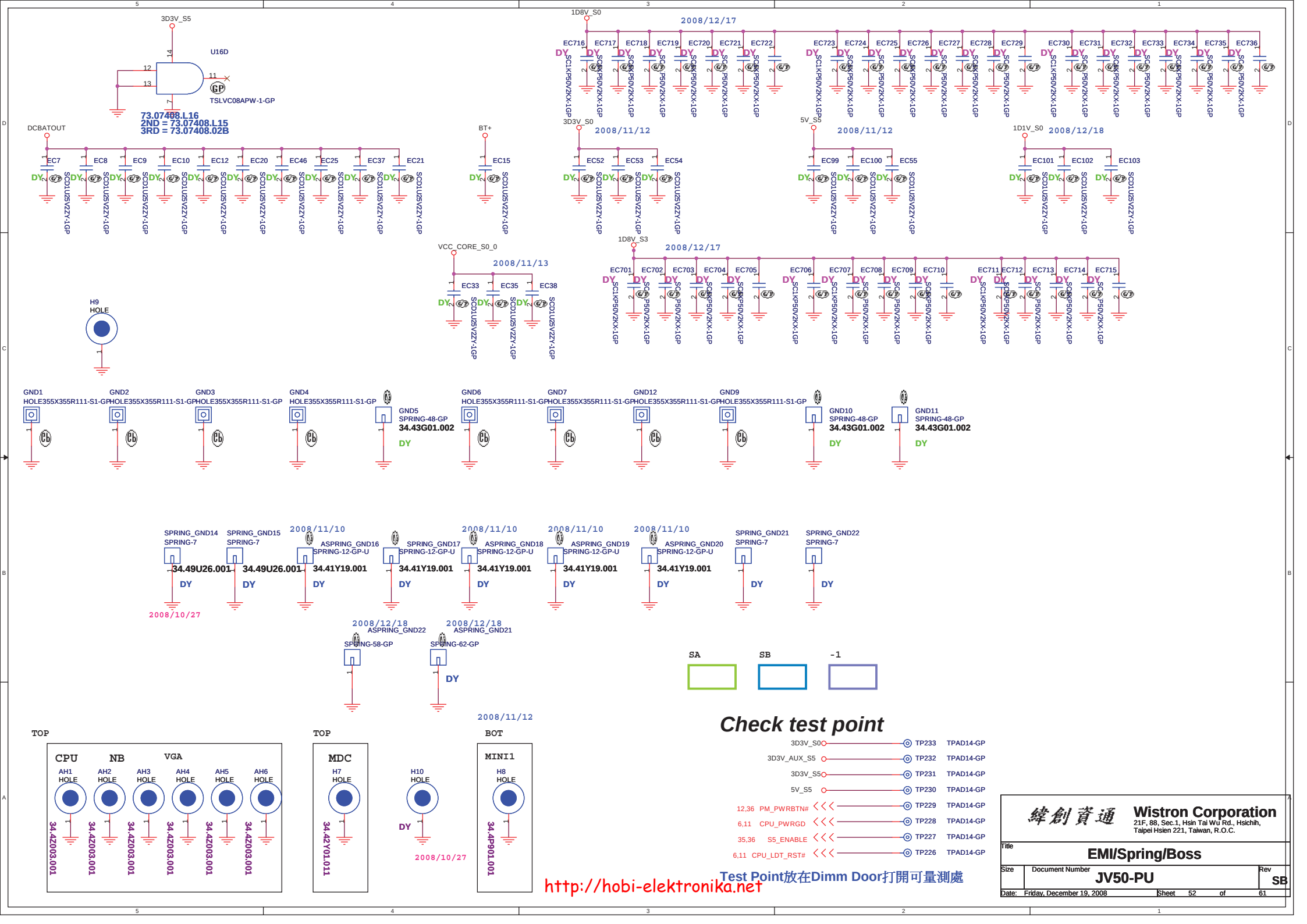


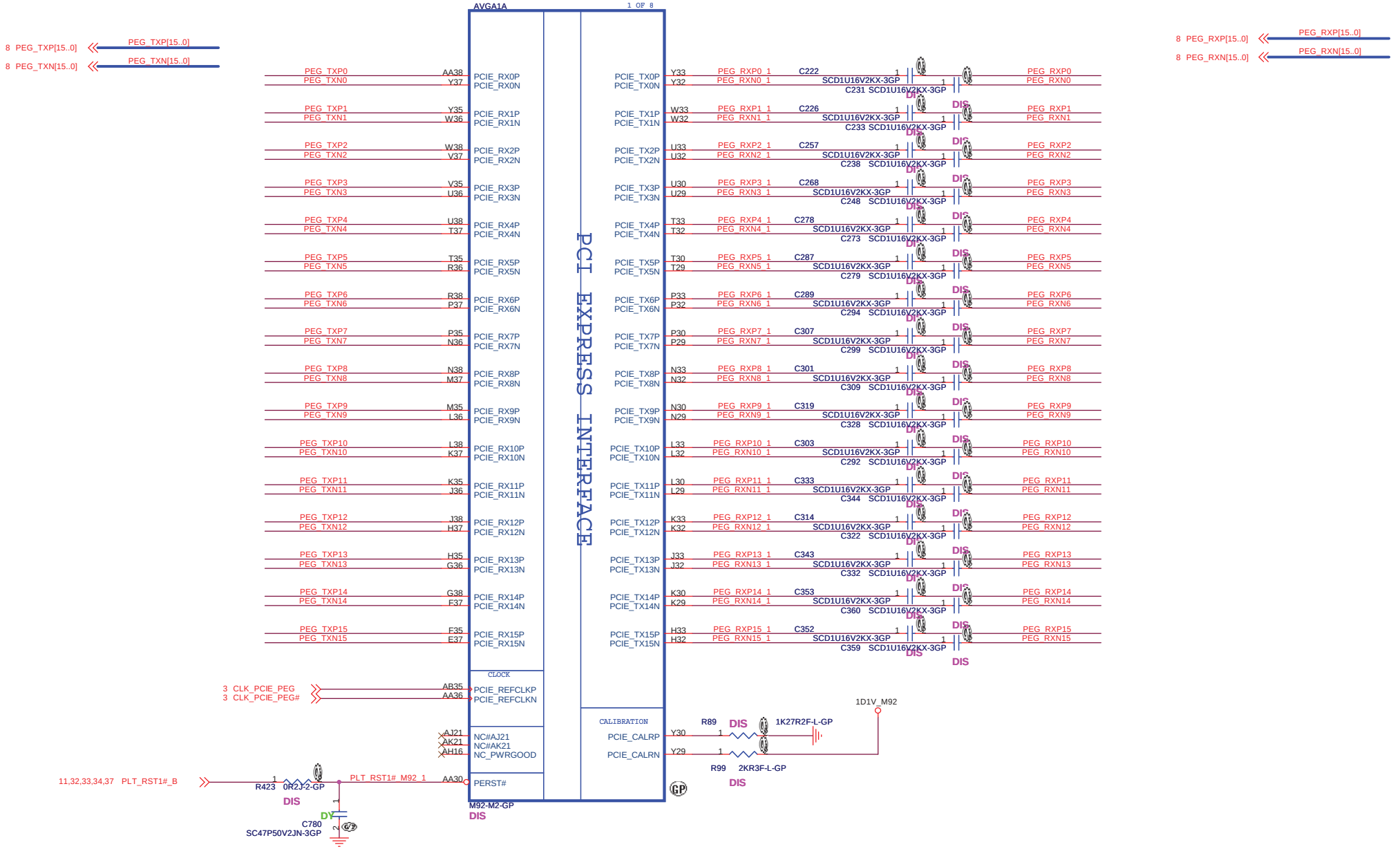
BATTERY CONNECTOR



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AD/BATT CONN	
Size	Document Number JV50-PU	Rev SB
Date: Friday, December 19, 2008	Sheet 51 of 61	


3D3V_S5
U16D
TSLVC08APW-1-GP
73.07408.L16
2ND = 73.07408.L15
3RD = 73.07408.02B
1D8V_S0
2008/12/17
DCBATOUT
BT+
3D3V_S0
2008/11/12
5V_S5
2008/11/12
1D1V_S0
2008/12/18
VCC_CORE_S0_0
2008/11/13
1D8V_S3
2008/12/17
H9
HOLE
GND1
GND2
GND3
GND4
GND5
SPRING-48-GP
34.43G01.002
DY
GND6
GND7
GND12
GND9
GND10
SPRING-48-GP
34.43G01.002
DY
GND11
SPRING-48-GP
34.43G01.002
DY
SPRING_GND14
SPRING-7
34.49U26.001
DY
2008/10/27
SPRING_GND15
SPRING-7
34.49U26.001
DY
2008/11/10
ASPRING_GND16
SPRING-12-GP-U
34.41Y19.001
DY
SPRING_GND17
SPRING-12-GP-U
34.41Y19.001
DY
2008/11/10
ASPRING_GND18
SPRING-12-GP-U
34.41Y19.001
DY
2008/11/10
ASPRING_GND19
SPRING-12-GP-U
34.41Y19.001
DY
2008/11/10
ASPRING_GND20
SPRING-12-GP-U
34.41Y19.001
DY
SPRING_GND21
SPRING-7
DY
SPRING_GND22
SPRING-7
DY
2008/12/18
ASPRING_GND22
SPRING-58-GP
2008/12/18
ASPRING_GND21
SPRING-62-GP
DY
2008/11/12
SA
SB
-1
Check test point
3D3V_S0 TP233 TPAD14-GP
3D3V_AUX_S5 TP232 TPAD14-GP
3D3V_S5 TP231 TPAD14-GP
5V_S5 TP230 TPAD14-GP
12,36 PM_PWRBTN# TP229 TPAD14-GP
6,11 CPU_PWRGD TP228 TPAD14-GP
35,36 S5_ENABLE TP227 TPAD14-GP
6,11 CPU_LDT_RST# TP226 TPAD14-GP
TOP
CPU
NB
VGA
AH1 HOLE
AH2 HOLE
AH3 HOLE
AH4 HOLE
AH5 HOLE
AH6 HOLE
34.4Z003.001
TOP
MDC
H7 HOLE
34.42Y01.011
H10 HOLE
DY
2008/10/27
BOT
MINI1
H8 HOLE
34.4P901.001
http://hobi-elektronika.net
Test Point放在Dimm Door打開可量測處
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI/Spring/Boss
Size
Document Number
JV50-PU
Rev
SB
Date: Friday, December 19, 2008
Sheet 52 of 61



M92

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: M92 PCIE

Size: A3 | Document Number: JV50-PU | Rev: SB

Date: Friday, December 19, 2008 | Sheet 53 of 61

Layout notice:
It should be pleace near HDMI connector

DVPDATA [3:2:1:0] for VRAM type selection H/W strap
Should provide VRAM Table for VBios request

2008/10/27

DVPDATA [3:0]
0100 512MB Hynix-H5PS1G63EFR-20L (500MHz)
1000 512MB Samsung-K4N1G164QE-HC20 (500MHz)
1100 512MB QIMONDA HYB18T1G161C2F-20 (500MHz)

It's strap for GDDR3-136ball
Need to Clarify

Back Bias (body bias) which minimizes power consumption in battery modes.
PD = Disable
PU = Enable

VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)

Depending on OSC used select voltage divider resist values R25 R70 to ensure XTALIN voltage level of 1.8V

2008/12/17 SB

82.30034.421

2008/11/07
2008/11/05

2008/11/04

2008/11/03

2008/11/10

2008/11/12

2008/12/17
2008/12/18

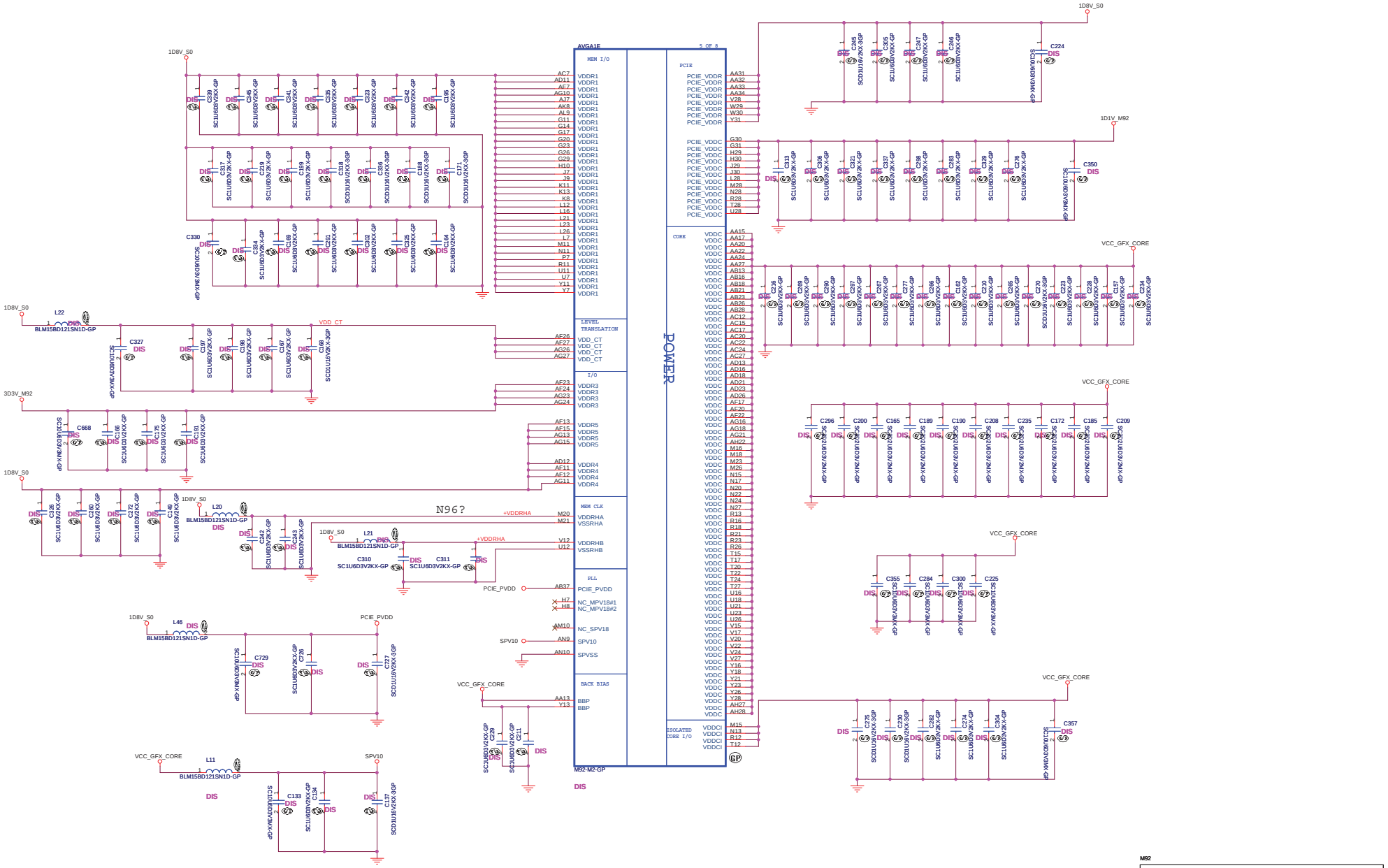
2008/12/17

2008/11/07

84.2N702.D31
2ND = 84.2N702.I31

84.T3904.C11
2ND = 84.03904.L06

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	M92 IO
Size A2	Document Number JV50-PU
Rev	SB
Date: Friday, December 19, 2008	Sheet 54 of 61



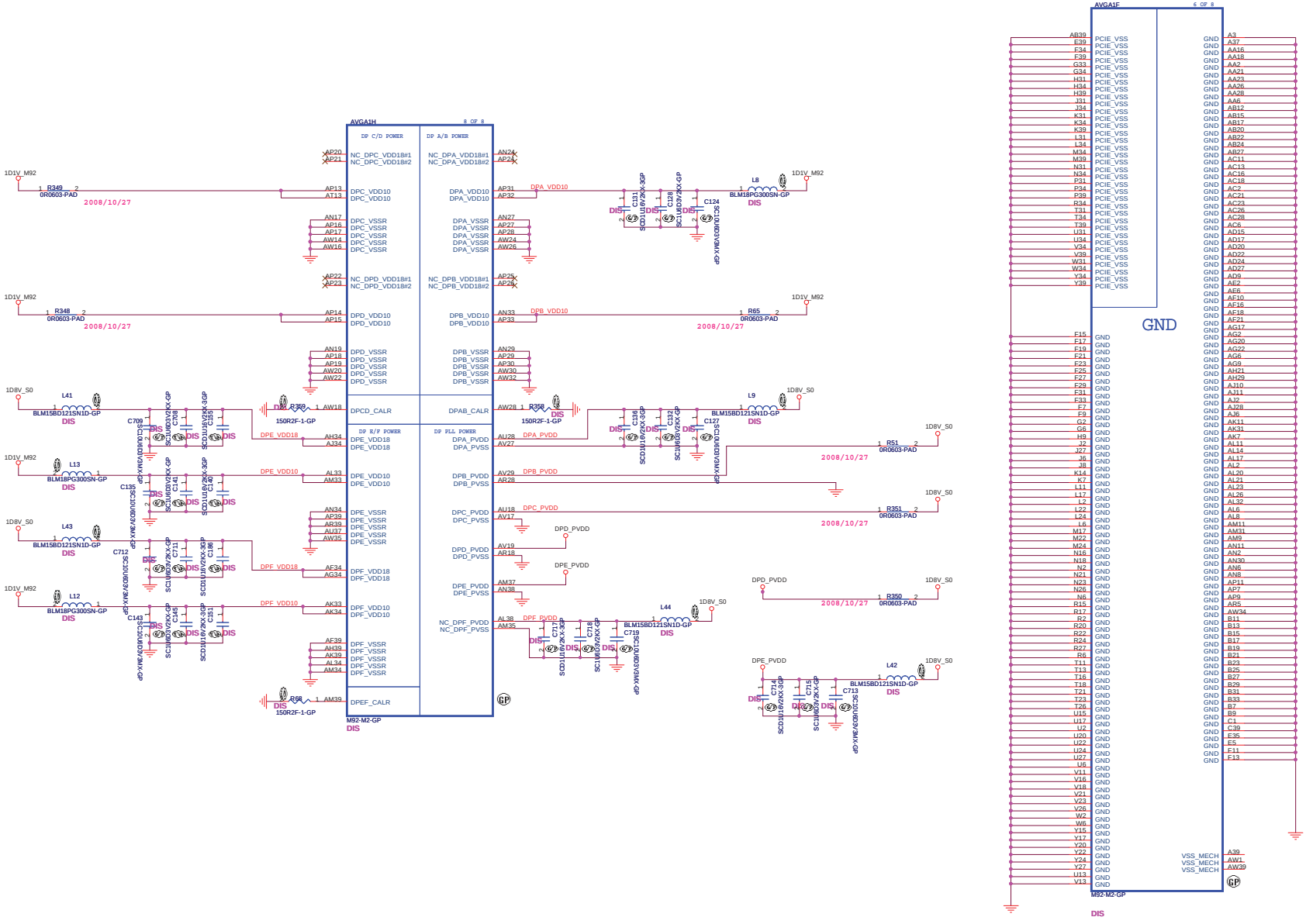
M92

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: M92 POWER

Size	Document Number	Rev
A2	JV50-PU	SB

Date: Friday, December 19, 2008 Sheet 55 of 61



M92

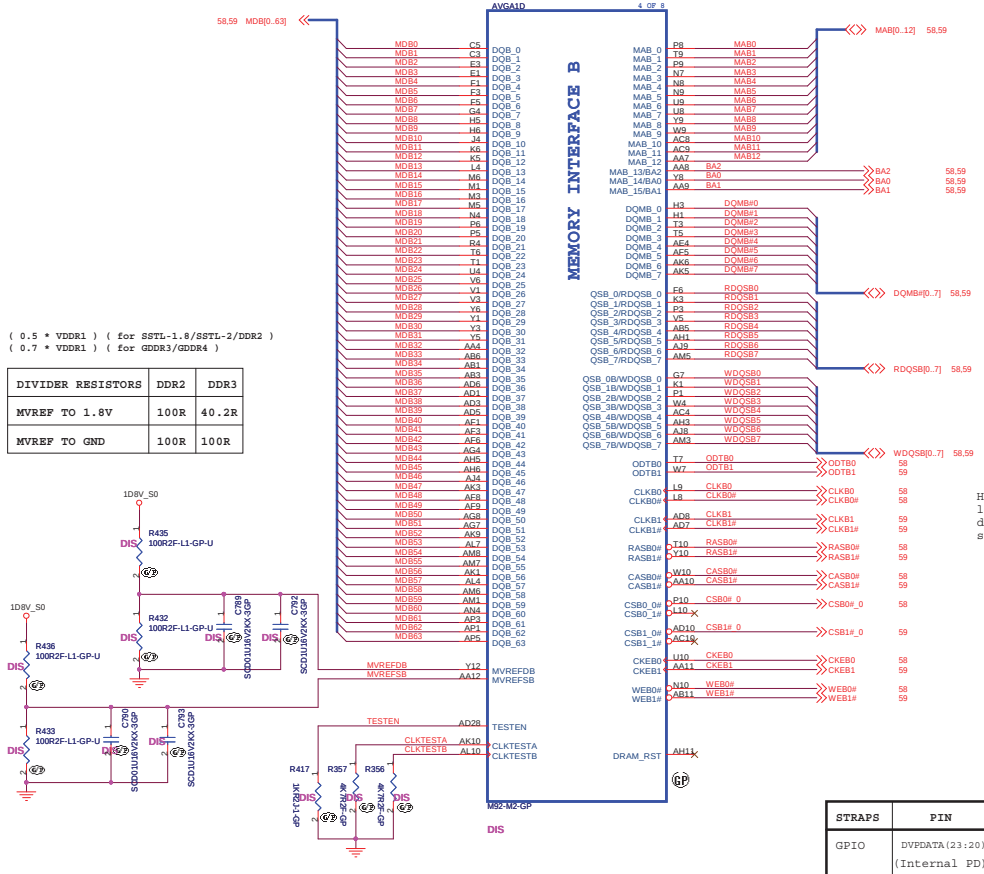
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DP POWER_GND**

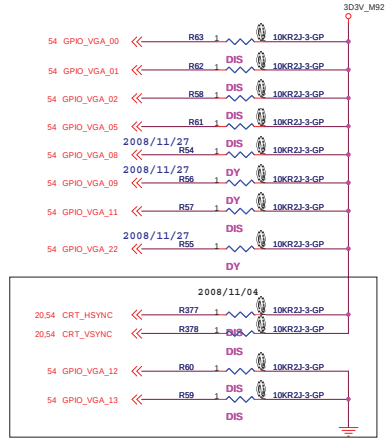
Size	Document Number	Rev
A2	JV50-PU	SB

Date: Friday, December 19, 2008 Sheet 56 of 61

M92-M2 uses memory group B only



DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R



HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.

STRAPS	PIN	DESCRIPTION
GPIO	DVPDATA(23:20) (Internal PD)	Initialization Behavior: This signal is input during reset (no reference clock is required). After reset, the default state is output low (0 V). The signals above can be left unconnected if not used.

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO , GPIO21_BB_EN

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x			
2GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
4GB	x		Pm25LV010A	0101

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	1
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s	1
AC_BATT	GPIO5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	
ROMSO	GPIO8	BIF_CLK_PM_EN Serial ROM Output from ROM	0
ROMSI	GPIO9	VGA ENABLED Serial ROM Input to ROM	0
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X
PWRCNTL_[1,0]	GPIO[15,20]	Power control signals to control the core voltage regulator	
BB_EN	GPIO21	Back Bias (body bias) which minimizes power consumption in battery modes. 0V = Disable 3D3V = Enable	0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	1
CCBYPASS	GENERICC		0

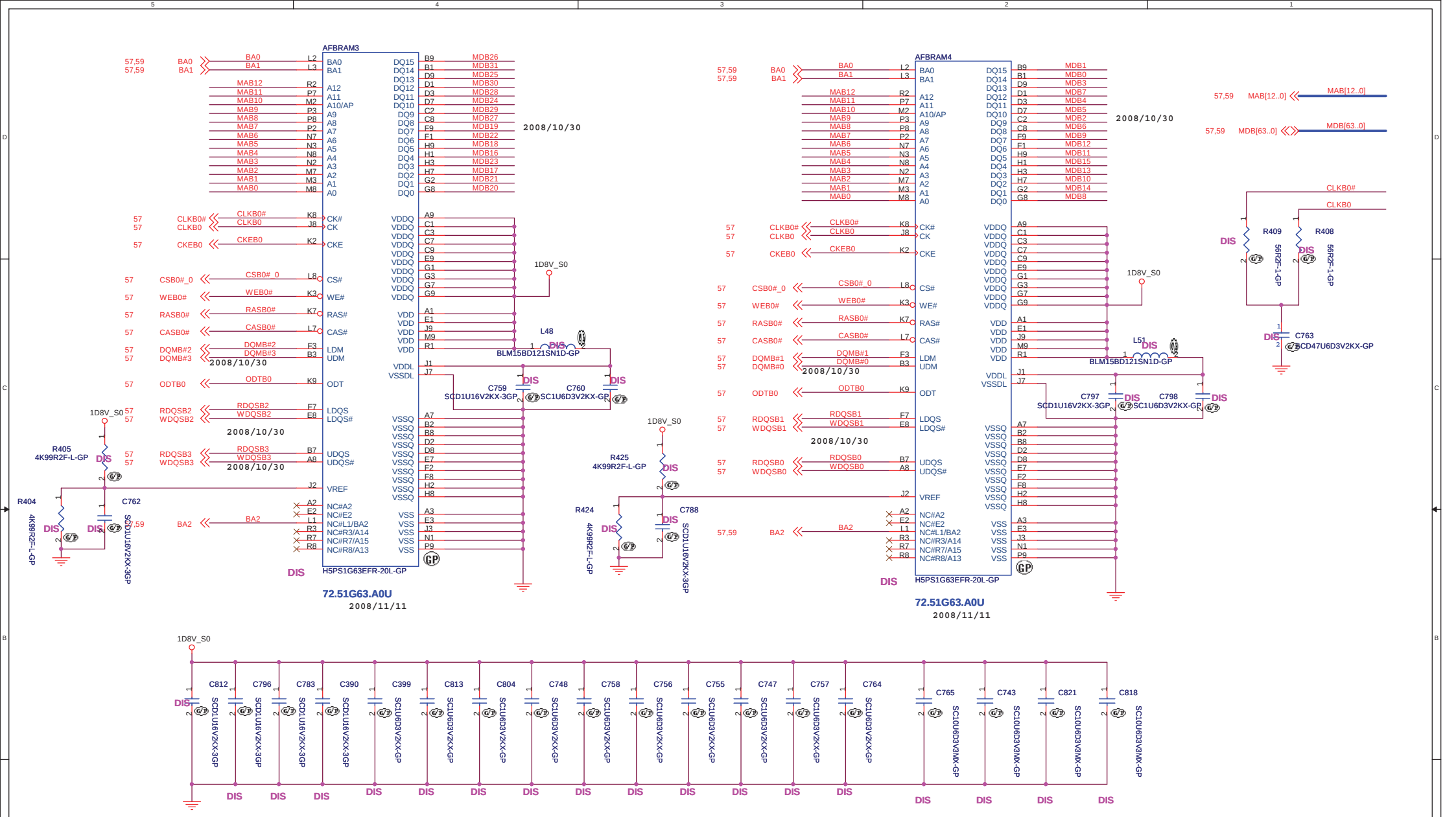
M92

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Memory / Straps

Size: A2 | Document Number: JV50-PU | Rev: SB

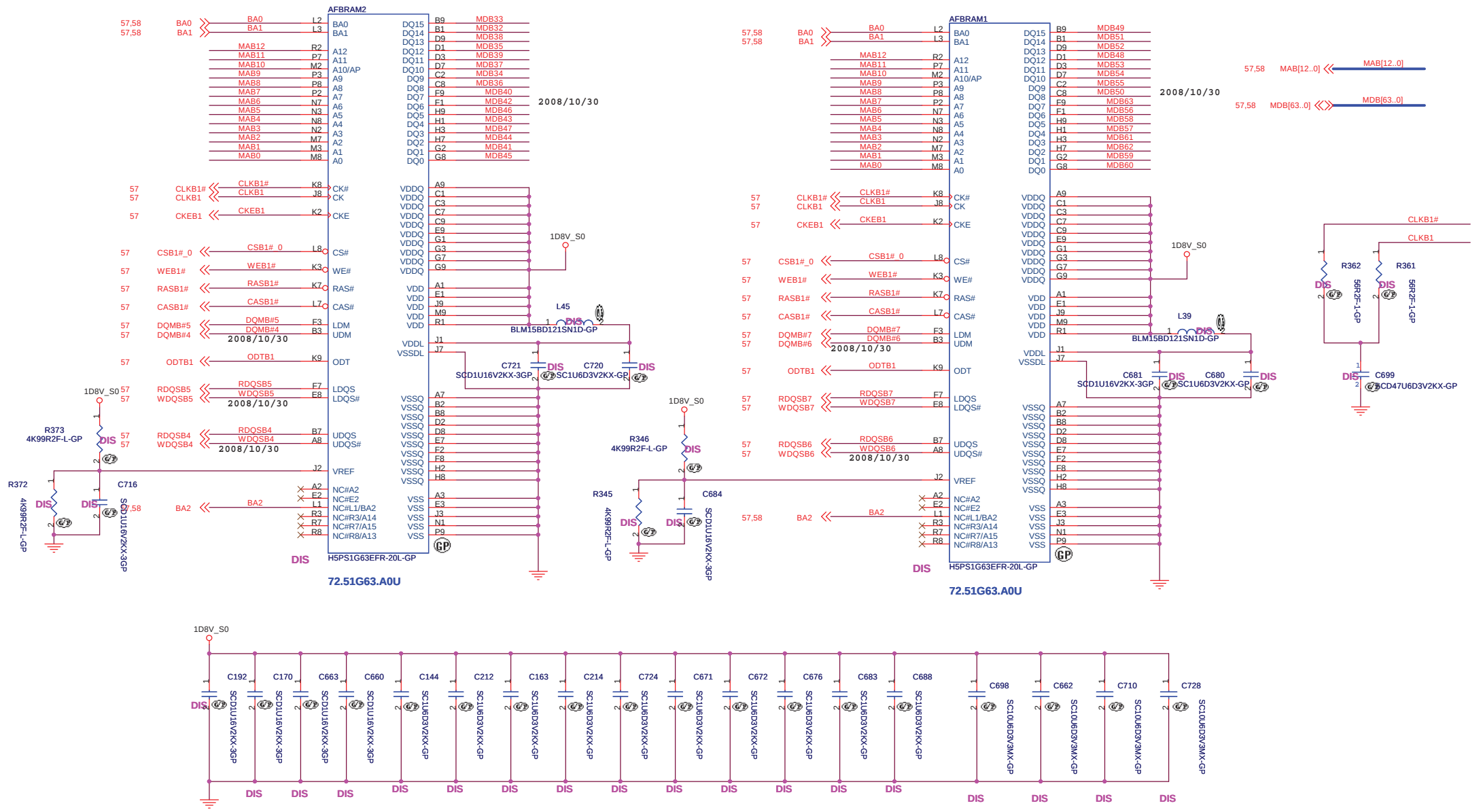
Date: Friday, December 19, 2008 | Sheet 57 of 61



M92

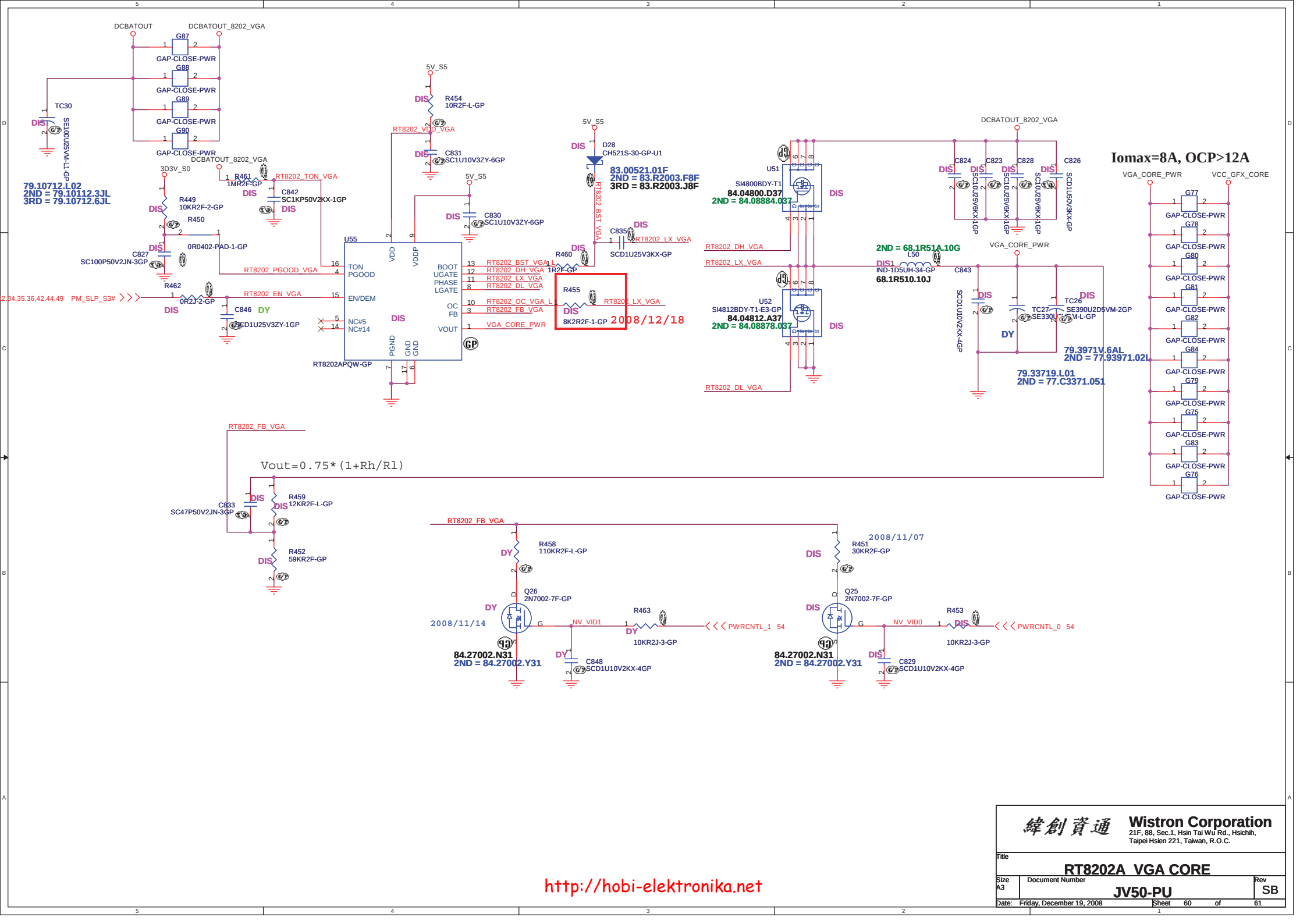
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR2 B0		
Size: A3	Document Number: JV50-PU	Rev: SB
Date: Friday, December 19, 2008	Sheet 58 of 61	



M92

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**M92 DDR2 B1**	
Size A3	Document Number **JV50-PU**	Rev **SB**
Date: Friday, December 19, 2008	Sheet 59 of 61	


DCBATOUT
DCBATOUT_8202_VGA
G87
G88
G89
G90
GAP-CLOSE-PWR
TC30
SE100U25VM-L1-GP
79.10712.L02
2ND = 79.10112.3JL
3RD = 79.10712.6JL
3D3V_S0
R461
1MR2F-GP
RT8202_TON_VGA
C842
SC1KP50V2KX-1GP
R449
10KR2F-2-GP
R450
0R0402-PAD-1-GP
C827
SC100P50V2JN-3GP
RT8202_PGOOD_VGA
R462
0R2J-2-GP
PM_SLP_S3#
C846
SCD1U25V3ZY-1GP
U55
TON
PGOOD
EN/DEM
NC#5
NC#14
VDD
VDDP
PGND
GND
BOOT
UGATE
PHASE
LGATE
OC
FB
VOUT
RT8202_EN_VGA
RT8202_OC_VGA_L
RT8202_FB_VGA
VGA_CORE_PWR
RT8202APQW-GP
5V_S5
R454
10R2F-L-GP
RT8202_VDD_VGA
C831
SC1U10V3ZY-6GP
C830
SC1U10V3ZY-6GP
D28
CH521S-30-GP-U1
83.00521.01F
2ND = 83.R2003.F8F
3RD = 83.R2003.J8F
RT8202_BST_VGA
C835
SCD1U25V3KX-GP
RT8202_LX_VGA
R460
1R2F-GP
R455
8K2R2F-1-GP
2008/12/18
U51
SI4800BDY-T1
84.04800.D37
2ND = 84.08884.037
U52
SI4812BDY-T1-E3-GP
84.04812.A37
2ND = 84.08878.037
RT8202_DH_VGA
RT8202_LX_VGA
RT8202_DL_VGA
C824
C823
C828
C826
SC10U25V6KX1GP
SCD1U50V3KX-GP
L50
IND-1D5UH-34-GP
68.1R510.10J
2ND = 68.1R51A.10G
C843
SCD1U10V2KX-4GP
TC26
TC27
SE390U2D5VM-2GP
SE330U2D5VM-L-GP
79.3971V.6AL
2ND = 77.93971.02L
79.33719.L01
2ND = 77.C3371.051
Iomax=8A, OCP>12A
VGA_CORE_PWR
VCC_GFX_CORE
G77
G78
G80
G81
G82
G84
G79
G75
G83
G76
Vout=0.75*(1+Rh/Rl)
C833
SC47P50V2JN-3GP
R459
12KR2F-L-GP
R452
59KR2F-GP
R458
110KR2F-L-GP
Q26
2N7002-7F-GP
2008/11/14
NV_VID1
R463
10KR2J-3-GP
PWRCNTL_1 54
84.27002.N31
2ND = 84.27002.Y31
C848
SCD1U10V2KX-4GP
R451
30KR2F-GP
2008/11/07
Q25
2N7002-7F-GP
NV_VID0
R453
10KR2J-3-GP
PWRCNTL_0 54
C829
SCD1U10V2KX-4GP
http://hobi-elektronika.net
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RT8202A VGA CORE
Size
A3
Document Number
JV50-PU
Rev
SB
Date: Friday, December 19, 2008
Sheet 60 of 61

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HISTORY**

Size	Document Number	Rev
A3	JV50-PU	SB

Date: Friday, December 19, 2008 Sheet 61 of 61